

EARTH PEOPLE TECHNOLOGY, Inc

CycloFlex DEVELOPMENT SYSTEM User Manual

The CycloFlex is an FPGA development board that is designed for the intermediate user with some experience designing FPGA projects. This board provides a powerful platform for developing and debugging programmable logic code. It has been designed from the ground up to provide the functionality needed for the demanding projects from todays students and hobbyists. The board provides a convenient, user-friendly work flow by connecting seamlessly with Altera's Quartus Prime Lite software. The user will develop the code in the Quartus environment on a Windows Personal Computer. The programmable logic code is loaded into the FPGA using only the Quartus Programmer tool.

The core of the CycloFlex is the Altera Cyclone 10 FPGA. This powerful chip has 16,000 Logic Elements and 504 Kbits of Memory. The Cyclone 10 is easily scalable from the entry level college student to the most advanced projects like an audio sound meter with FFT.

Circuit designs, software and documentation are copyright © 2025, Earth People Technology, Inc



Microsoft and Windows are both registered trademarks of Microsoft Corporation. Altera is a trademark of the Altera Corporation. All other trademarks referenced herein are the property of their respective owners and no trademark rights to the same are claimed. <u>http://www.earthpeopletechnology.com/</u>

Contents

| 1 2 | Intro User | oduction Setup | 4 5 |
|--------|---------------|------------------------------------|--------|
| | 2.1 | Getting Started with the CycloFlex | 7 |
| 3 | Cyc | oFlex Description | 6 |
| | 3.1 | PCB Footprint | 6 |
| | 3.2 | Functional Block Diagram | 6 |
| | 3.3 | CycloFlex Specifications | 7 |
| | 3.4 | Cyclone 10 FPGA 2 | 8 |
| | 3.5 | Power Supply 2 | 8 |
| | 3.6 | Clock Domain | 2 |
| | 3.7 | Digital I/Os | 4 |
| | 3.8 | LEDs | 8 |
| | 3.9 | RGB LED | 3 |
| | 3.10 | Seven Segment LED Displays | 6 |
| | 3.11 | PushButtons | 3 |
| | 3.12 | Serial Flash | 6 |
| | 3.12 | .1 S25FL127S Command Set | 0 |
| | 3.12 | .2 Read Identification (RDID 9Fh) | 1 |
| | 3.12 | .3 Register Access commands | 4 |
| | 3.13 | Power Input | 5 |



| | 3.14 | Com | nmunications Interface | 65 |
|-------|--------|--------|--|-----|
| | 3.14 | .1 | CONNECT LED | 71 |
| | 3.14 | .2 | Active Host Communications | 72 |
| | 3.14 | .3 | CONF DONE LED | 73 |
| | 3.15 | JTA | G Interface | 74 |
| | 3.16 | Cont | figuration Flash Programming | 80 |
| 4 | Pow | vering | the CycloFlex | 86 |
| 5 | EPT | Driv | vers | 88 |
| | 5.1 | USB | B Driver | 89 |
| 6 | Insta | alling | Quartus | 92 |
| 6.1.1 | | 1 | Downloading Quartus | 92 |
| | 6.1.2 | 2 | Quartus Installer | 99 |
| 7 | Con | npilin | g and Synthesizing the FPGA Project | 110 |
| | 7.1 | Setti | ng up the Project and Compiling | 110 |
| | 7.1. | 1 | Selecting Pins and Synthesizing | 126 |
| 8 | Con | figuri | ing the FPGA | 139 |
| | 8.1 | JTA | G Direct Programming of the FPGA | 140 |
| | 8.2 | Cont | figuration Flash Programming of the FPGA | 155 |
| | 8.3 | Crea | ting a *.pof File for Configuration Flash | 181 |
| G | enerat | ion o | f *.pof file from *.sof file for Altera FPGA | 181 |





• Please Note: The CycloFlex Does Not Contain On Board Programmer. JTAG Programming and Configuration Flash Programming must be performed by external Programmer Purchased Separately.

1 Introduction

The CycloFlex is an FPGA Development Board based on the Cyclone 10 FPGA. Core of the board is the Cyclone 10 chip. This chip is a powerful mid-range FPGA from Altera. It provides a high density sea of programmable gates, on-board resources and general purpose I/O's. The CycloFlex includes high speed USB to SPI communications which allow data transfers up to 4MegaBits per second. The board includes three Seven Segment LED Displays which gives the user more options for code debugging than simple LEDs. The CycloFlex also includes two pushbuttons, one RGB LED and Eight traditional Green LEDs and of course loads of General



Purpose Inputs/Outputs. There is an on board 50MHz oscillator that feeds the internal PLLs of the Cyclone 10.

2 User Setup

The CycloFlex is ready to go straight out of the box. Just connect power from either a USP Port (from PC/Laptop), USB-C Charger (10Watt to 45Watt Charger allowed) or +5 to 5.5 VDC through barrel connector.



Next, connect a JTAG Blaster or Altera USB Blaster to J2 for programming the Cyclone 10 chip.





Then, write some code, synthesize, and program the chip.



See Programming and Configuration Section for details about programming the CycloFlex board.

Page



2.1 Getting Started with the CycloFlex

The CycloFlex board comes pre-loaded with the EPT_System_Demo HDL project in the FPGA. This project allows the user to test out the functions of the Active Host API and the board hardware.



To test drive the application, connect the CycloFlex to the Windows PC using a USB-C cable. Load the driver for the board. See the section "EPT Drivers" for instructions on loading the CycloFlex driver. If the USB driver fails to load, the Windows OS will indicate that no driver was loaded for the device. In the case of the failed USB driver, try rebooting the PC and following the steps in the EPT Drivers section of this User Manual.

Page





Next, open a Windows Explorer browser.

 $Browse \ to \ the \ Projects_ActiveHost\EPT_System_Demo\EPT_System_Demo\bin\Debug\ folder \ on \ the \ CycloFlex_FPGA_SYSTEM_PROJECT_x.x_DVD.$



Double click on the EPT_System_Demo.exe. The application should load with a Windows form.





With the application loaded, select the FPGA board (EPT CycloFlex x) from the dropdown combo box and click on the "Open" button.



| 骎 EPT_System_Demo | | | |
|--|-----------------------------------|-------------------------------|----------------------|
| CycloFlex Board 0 | LED Cortal Dn On Shift Left | LED 3 LED 4 LED 5 On On On | LED 6 LED 7 LED 8 LE |
| Transfer LoopBack Controls | Come Core | onic high Coon of | PushButton |
| Send Byte: 255 Addres | ss 2 Receive Byte | ^ | 'Switches |
| Multiple Byte: 55 66 77 88 Multi Byte | | Rst | Rst |
| GPIO Controls | | | |
| Start | | | |

When the EPT System Demo software has properly accessed the board, the "Device Connected" label will appear.



| 🖳 EPT_System_Demo | | | | |
|--|----------------|--------------------|---------------------------|-------------------------------------|
| CycloFlex Boar V Dev Open Close | rice Connected | On On On | LED 4 LED 5 LI On On (| ED 6 LED 7 LED 8 LE On On On |
| Transfer LoopBack Co Send Byte: 255 | Address 2 Rea | Shift Left Shift R | ight Count Up | Count Dwn PushButton Switches |
| Byte Multiple Byte: 55 66 | 77 88 | | _ | Rst |
| Multi Byte | | F | Rst | |
| GPIO Controis | | | | •••• |
| | | | | 1 |
| Start | A 10000 | | CONE DONE | |

In the "Transfer LoopBack Controls" Group, leave the Address set at 2.

To exercise the Single Byte Transfer EndTerm, click the "Byte" button in the Transfer Controls group.



| 💀 EPT_System_Demo | | |
|---|---|---------|
| CycloFlex Boar Device Connected Open Close Shift Left | 2 LED 3 LED 4 LED 5 LED 6 LED 7 LED 8 On On On On On On On Shift Right Count Up Count Dwn | E V |
| Transfer LoopBack Controls Send Byte: 255 Address 2 Receive Byte Byte | ■ PushButton Switches | RGB LED |
| Multiple Byte: 55 66 77 88 Multi Byte | Rst | On |
| GPIO Controls | | |
| Start | CONF_DONE I I I I I I I I I I I I I I I I I I I | |

The byte in the drop down box will be transmitted to the CycloFlex. Then, the CycloFlex will receive the byte and re-send it back to the Host PC to be displayed in the "Receive Byte" Text Box.



| 🖳 EPT_System_Demo | | | |
|--|------------------------|--|---|
| CycloFlex Boar V Device Con Open Close Transfer Loop Back Controls Send Byte: 255 | Address 2 Receive Byte | 2 LED 3 LED 4 LED 5 L n On On On Shift Right Count Up . 255 | ED 6 LED 7 LED 8 LED On On On E Count Dwn PushButton Switches RGI |
| Multiple Byte: 55 66 77 88 Multi Byte | | Rst | Rst |
| GPIO Controls | | | |
| Start | | CONF_DONE | |

The user can change the byte in the "Send Byte:" Text Box and attempt the loopback again. This box is in decimal format, so the byte is limited to 0 to 255 decimal. In hexadecimal, it is 0x00 to 0xff.

Type in several numbers separated by a space and less 256 into the "Multiple Byte" textbox.



| 🖳 EPT_System_Demo | | | |
|--|---|--|--|
| CycloFlex Boar V Device Connected | LED Control LED 1 LED On On Shift Left | 2 LED 3 LED 4 LED 5 I On On On Shift Right Count U | LED 6 LED 7 LED 8 LED On On On E Count Dwn |
| Send Byte: 255 Address | 2 Receive Byte | , 255 | PushButton 'Switches RGI |
| Multiple Byte: 55 66 77 88 Multi Byte | | Rst | Rst |
| GPIO Controls | | | |
| Start | | | |
| | DOOO6 | CONF_DONE | 3 💭 ; 10 11 ²⁰ (2010) |

Then hit the "Multi Byte" button. The numbers appear in the "Receive Byte" textbox.



| 🖳 EPT_System_Demo | | |
|--|---|---|
| CycloFlex Boar V Device Co Open Close | Inected LED Cortect LED 1 LED 2 LED 3 LED 4 LED 5 LED 6 LED 7 LED 8 On On O | - |
| Transfer LoopBack Controls | PushButton | |
| Send Byte: 255 Byte | Address 2 Receive Byte . 55, 66, 77, 88 Switches | |
| Multiple Byte: 55 66 77 88 | Rst | |
| Multi Byte | Rst | |
| GPIO Controls - | | |
| | | • |
| Start | | |
| Infinite | | |



Ensure that the "Heartbeat" function is displayed on the Green User LEDs (repeating sweep of the LEDs)



Under LED Controls, press the "Shift Right" button, Notice the change in direction of the LED Heartbeat.



| 🖳 EPT_System_Demo | |
|---|--|
| CycloFlex Boar Device Connected LED CortLED 1 Open Close Shift Transfer LoopBack Controls Send Byte: 255 Address 2 Byte Byte Multiple Byte: 55 66 77 88 5 | LED 2 LED 3 LED 4 LED 5 LED 6 LED 7 LED 8 On On On On On On On On On On On t Left Shift Right Count Up Count Dwn yte . 55, 66, 77, 88, 90, 195, 126, 32, 8, 90, 195, 126, 126, 32, 8, 90, 195, 126, 48 Black Black |
| Multi Byte | Rst |
| | |
| Start Infinite | |

Ensure that the "Heartbeat" function changes direction.





The user can click on the other buttons in the LED Controls Group to see the change to LED pattern.



Next, under the "RGB LED Controls", click the "Blink" button

| 🖶 EPT_System_Demo | | | | |
|--|---|---|----------------|--|
| CycloRex Boar Device Connected Copen Close Transfer LoopBack Controls Send Byte: 255 Byte | ED Cor ⁺ (ED 1 LED 2 LED 3 L On On On Shift Left Shift Riv Receive Byte | ED 4 LED 5 LED 6 LED 7 On On On On On aht Count Up Count D PushButto Switches | n LED Displays | A v Disp 3 Shift Left Shift Right Blink Stop Blink an Reset Rel |
| Multiple Byte: 55 66 77 88 Multi Byte GPIO Controls | R | st | Rst On On Or | Rst |
| Start | 000 | | | |
| • Infinite | CONNECT | | | |
| ○ Single | | | | JTAG |



Ensure that the RGB LED goes through its full test of Red, Blue and Green colors



Under the "LED Displays" group box, the characters "EPA" will be displayed on the three LED Displays. Locate the three displays on the CycloFlex in the upper right corner.





Click on the "Shift Left" button on the LED Displays group.

🖳 EPT_System_Demo





Take note that the LED Display Characters shift to the Left at a 1 second rate.



To exercise the Block Transfer EndTerm, click the "Start" button in the GPIO Controls group. The CycloFlex will sample the state of selected Input pins of the FPGA that is connected to a board edge connector. The System Demo Window will display the results of each pin, Hi or Lo





| 🖷 EPT System Demo | – o x |
|--|--|
| EPI_System_Demo LED Corrticion CycloRex Boar >> Device Connected LED Corrticion Open Close Transfer LoopBack Controls Shift Right Send Byte: 255 Address 2 Receive Byte Switches Multiple Byte: 55 66 77 88 Multi Byte Rst | LED Displays E V P V A V Shift Left Disp 1 Disp 2 Disp 3 Stop RGB LED Controls Red Blue Green Reset On On On Rst |
| GPIO Controls Start Infinite Single | HI HI HI HI HI HI HI HI HI HI |

The results of each pin are displayed next to the image of the CycloFlex in separate buttons.



| 🖳 EPT_System_Demo | | | | | _ | × |
|--|-------------------------------|------------------|--------------------------|---|---|----|
| | LED Control | | LED Displays | | | |
| Cycloriex Boar V Device Connected | On On On On On O | On On On On | | Shift Left | | |
| Open Close | | | E ~ P ~ A ~ | Shift Right | | |
| | Shift Left Shift Right Co | unt Up Count Dwn | Dian 1 Dian 2 Dian 2 | Blink | | |
| Transfer LoopBack Controls | | PushButton | | Stop | | |
| Send Byte: 255 Address | 2 Heceive Byte | Switches | RGB LED Controls | | | |
| Byte | | | | Blink | | |
| | | | Red Blue Green Reset | Roll | | |
| Multiple Byte: 55 66 77 88 | _ | Rst | On On On Bet | | | |
| Multi Byte | | 20 | | | | |
| | Hst | | | | | |
| GPIO Controls | | | | | | |
| t 🕇 💶 | | 1 1 1 1 1 | | | | |
| 1 1 | | | | | | |
| | | | | and the second se | | |
| | | | DISPI DISP2 DISP3 | | | |
| | | | า อัฐธิสิสิสิติของสีชิชี | | | |
| X | | | | 10 | | |
| Stop | THE PARTY IS NOT THE | | | | | |
| 200 | 00006-11-1 | - [] - 1 | | Hi Hi | | |
| | TA 12C SENSOR | INE E S | | Lo | | |
| | | | | T | | |
| - state | | unumumum | | 0 - 1 | | |
| | CONNECT (1) | 1 | LED DISECAY | | | |
| | PER INTER STATE | | | | | |
| | 2.5 | | | | | |
| | | • II | | | | |
| | EARTHPEOPLE" I-J | | JTAG | | | |
| | TECHNOLOG | | PROGRAMING T | | | |
| | | | | | | 0 |
| and the second s | | | in the PLASE | C | | 31 |
| A BAD | | | | | | |
| UST | | Effect of 1 | 1 4 | | | |
| 1.30 | | | | | | |
| | | | 1 100 | | | |
| | | | | 1 | | |
| T ALL ALL | | | | | | |
| 1 | | | | | | |
| | 10 1 . | - 10 | SERIAL FLASH | | | |
| 10 Mar | | | JIAG - | | | |
| | | | | | | |
| | | | | | | |
| | un un tel tel tel tel tel tel | | | | | |

Selected inputs are attached to the User LEDs, the RGB LED, and the LED Displays. So, a mixture of alternating Hi and Lo indications is normal. The user can make contact with the GPIO connector pins at the bottom of the board at the XIO_4. Notice the GPIO pins will move from Hi



| | | | | <i>L</i> 0. | | | |
|-----------------------------------|------------------------------------|----------------------------------|----------------------|----------------------|--|---|---|
| 🛃 EPT_System_Demo | | | | | | _ | × |
| CycloFlex Boar V Device Connected | LED Cortect 1 LED 2 LED On On O | 3LED 4 LED 5 LED 6 n On On On | LED 7 LED 8 On On | E V P V A V | Shift Left Shift Right | | |
| Transfer LoopBack Controls | Shift Left Shift | t Right Count Up C | Count Dwn | Disp 1 Disp 2 Disp 3 | Blink | | |
| Send Bite: 255 Address | 2 Receive Byte | A Sv | vitches | | Stop | | |
| Byte | - | | | RGB LED Controls | Blink | | |
| | | | | Red Blue Green Reset | Roll | | |
| Multiple Byte: 55 66 77 88 | | - | Rst | | | | |
| Multi Byte | | Rst | | | | | |
| Stop Stop Stop Single | | | | | SP3 B B C C C C C C C C C C C C C | | |

The user can also connect +3.3V or Ground using a jumper to any of the GPIO's in the board edge connector. Be sure NOT to connect +3.3V to a Ground pin or Ground to a +3.3V pin. Consult the Data Sheet for the location of the Inputs on the connectors.

This descibes the EPT System Demo Software for the CycloFlex Board. All source code for the FPGA and Host PC are available on the EPT_FPGA_SYSTEM_PROJECT_1.0_DVD. The following sections of this user manual can be used to determine how to make changes to the EPT System Demo FPGA code as well as the Visual C# project.

Page 25



3 CycloFlex Description

3.1 PCB Footprint

The PCB is 94mm x 65mm with four mounting holes (M2 metric screws) spaced as shown in the figure. These mounting holes are electrically isolated from all signals on the CycloFlex. The two connectors (USB and DC power) overhang the PCB by approximately 1mm in order to accommodate mounting within an enclosure.



26



3.3 CycloFlex Specifications

- Cyclone 10 10CL016 FPGA From Altera
- 16,000 Logic Elements, 504 Kbits of SRAM memory and four clock module PLLs;
- 4 Mbit On Board Configuration Flash
- 64 Inputs/Outputs available at connectors on board
- 8 Green User configurable LEDs 2 Pushbutton Switches
- Three Seven Segment LED Displays
- On Board Serial Flash
- Two Power options: Standard USB (+5V @ 2Amp) Using USB-C connector;
- 5mm Barrel Connector Accepts +5V @ 3Amp
- 50MHz Oscillator
- On board USB to Slave SPI Adapter for high speed communications



Page 27



3.4 Cyclone 10 FPGA

The CycloFlex includes the Altera 10CL016YE144C8G FPGA (Cyclone 10). It is an EQFP 144 pin package. The chip is optimized for low cost and low static power, making them ideal for high-volume and cost-sensitive applications. The Cyclone 10 is based on 20nm chip architecture from Intel. It has internal speed of 402MHz Clock Tree performance. The parameters for the 10CL016:

| Parameter | 10CL016 |
|---------------------------|---------|
| LEs (Logic Elements) | 16,000 |
| Block memory (Kb) | 504 |
| 18 x 18 multipliers | 56 |
| Phase-locked loops (PLLs) | 4 |
| Maximum I/O | 78 |

3.5 Power Supply

The CycloFlex board has three discrete power supplies on board.

- +3.3VDC
- +2.5VDC
- +1.2VDC

These supplies provide power for the FPGA and the various components on the board. The +2.5V and +1.2V supplies are only used internal to the board. The +3.3V supply is available to the user to power off board electronics. The +3.3V supply is available at the following User I/O connections.





+3.3V POWER SUPPLY

| Connector | Pin Number | Power Signal | Description |
|-----------|------------|--------------|------------------------|
| | | | |
| J8 | 9 | +3.3V | The User +3.3V pins |
| | 10 | +3.3V | of the connectors have |
| | | | full access to the |
| | | | Power Supply with No |
| | | | Current Limiting. The |
| | | | User must take |
| J11 | 9 | +3.3V | caution not to sink |



| | 10 | +3.3V | more than 1.5A from a combination of all +3.3V pins. |
|-----|----|--------|--|
| J14 | 1 | +3.3V | |
| J6 | 9 | GROUND | |
| | 10 | GROUND | |
| J7 | 9 | GROUND | |
| | 10 | GROUND | |
| J9 | 9 | GROUND | |
| | 10 | GROUND | |
| J10 | 9 | GROUND | |
| | 10 | GROUND | |
| J12 | 9 | GROUND | |
| | 10 | GROUND | |
| J14 | 2 | GROUND | |

The CycloFlex is designed to be operated from one of two different power sources:

- USB-C cable from Laptop/PC.
- +4.5 to +5.5 VDC supplied through the DC power jack.

This provides power for a high-efficiency switching regulator on-board to provide +3.3 VDC. The power supply provides reliable power under dynamic loads and high frequency switching internal to the FPGA.





The core of the +3.3VDC Power Supply is the Texas Instruments TPS54229 chip.



CycloFlex +3.3VDC Switching Power Supply

Page 31



The TPS54229 is a very stable synchronous buck converter. This allows it to provide a fast transient response. You can view this response here:



The +3.3VDC includes a 3.3uH Inductor capable of 3.2A RMS. Coupled with two 10uF 25V Ceramic Capacitors, this supply can deliver ultra stable load to the FPGA while at the same time providing power to User needs via the I/O connector pins. This supply provides a lot of power and takes up a small amount of real estate on the CycloFlex board.

3.6 Clock Domain

The CycloFlex provides an external clock domain to the Cyclone 10 FPGA, 50 MHz. The 50 MHz oscillator is Part Number: ASDMB-50.000MHZ-LC-T and is a +3.3VDC device that provides a high speed clock to the FPGA. It is a





CMOS device that provides a stable 50 MHz at \pm 50 ppm. This clock can be used directly in the user code or use it as an input to one of the PLL's internal to the FPGA. It is intended that this clock will drive the logic of the user code. If a different clock frequency is required in the user code, use the PLL scale up/down to produce the desired clocking.





The oscillator is held operational when the enable signal is high.

| Parameter | Min | Max | Units |
|------------------------------|-----|-----|-------|
| Overall Frequency Stability: | -50 | +50 | ppm |
| Operating Temperature: | 0 | +70 | °C |
| Output Load: | | 25 | pF |
| Supply Current | 9 | 16 | mA |

3.7 Digital I/Os

The CycloFlex has eight 10 pin headers that provide 64 digital Inputs and Outputs. All of the I/O's are +3.3 VDC only. All I/O's connect directly from the FPGA to one of the ten pin headers.





All I/O's are organized into separate banks of the FPGA. There are eight banks. These different banks provide different output speed technologies. Programmable Open Drain The optional open-drain output for each I/O pin is equivalent to an open collector output. If it is configured as an open drain, the logic value of the output is either high-Z or logic low. Use an external resistor





to pull the signal to a logic high. Programmable Bus Hold Each I/O pin provides an optional bushold feature that is active only after configuration. When the device enters user mode, the bushold circuit captures the value that is present on the pin by the end of the configuration. The bushold circuitry holds this pin state until the next input signal is present. Because of this, you do not require an external pull-up or pull-down resistor to hold a signal level when the bus is tristated. For each I/O pin, you can individually specify that the bus-hold circuitry pulls non-driven pins away from the input threshold voltage—where noise can cause unintended high-frequency switching. To prevent over-driving signals, the bus-hold circuitry drives the voltage level of the I/O pin lower than the VCCIO level. If you enable the bus-hold feature, you cannot use the programmable pull-up option. To configure the I/O pin provides an optional programmable pull-up resistor during user mode. The pull-up resistor weakly holds the I/O to the VCCIO level. If you enable the bus-hold feature. Programmable Pull-Up Resistor, you cannot use the bus-hold feature. Programmable Current Strength You can use the programmable current strength to mitigate the effects of high signal attenuation that is caused by a long transmission line or a legacy backplane.

To provide maximum flexibility to system designers, all FPGA I/O are intrinsically bidirectional. Based on the I/O direction specified in the configuration file, each I/O can be configured as input-only, output-only, or bidirectional. While the output buffer of a bidirectional I/O has always included a dynamic output enable signal, MAX 10 FPGAs also include an input buffer enable/disable capability. When an input buffer is dynamically disabled, the buffer presents its last known state to the FPGA core fabric, so that no inputs inside the FPGA are left floating.




| Connector | CycloFlex FPGA Label | |
|-----------|----------------------|--|
| J11 | XIO_1 | |
| J9 | XIO_2 | |
| J10 | XIO_3 | |
| J13 | XIO_4 | |
| J6 | XIO_5 | |
| J8 | XIO_6 | |
| J7 | XIO_7 | |
| J12 | XIO_8 | |



3.8 LEDs

The CycloFlex includes eight user LEDs and One RGB LED. These LEDs are fully controllable by the FPGA. They are directly driven from the FPGA. Each LED is connected to its own series







Resistor which provides current limiting. The LEDs are attached in a Current Sink configuration. This means the Anode of the LED is permanently connected to +3.3V via resistor. The Cathode is connected to Ground via a GPIO pin from the FPGA. Each LED Anode is connected with a 220 Ohm series resistor for each LED. This provides the following current through the LEDS

$$\begin{split} I_{LED} &= \text{Current flowing through the LED} \\ V_0 &= \text{Voltage applied to the LED} \\ V_F &= \text{Forward Voltage Drop of the LED} \\ R &= \text{Series Resistor Value} \\ I_{LED} &= \frac{V_0 - V_F}{R} \\ I_{LED} &= \frac{3.3V - 2.0V}{220} \\ I_{LED} &= 5.9 \text{mA} \end{split}$$

Page 39



| LED Number | CycloFlex Schematic Signal | LED Signal Name | Cyclone 10 Pin Number |
|------------|----------------------------------|-----------------|--------------------------|
| D2 | UB0 | USER_LEDS[0] | 10 |
| D3 | UB1 | USER_LEDS[1] | 32 |
| D4 | UB2 | USER_LEDS[2] | 33 |
| D5 | UB3 | USER_LEDS[3] | 42 |
| D10 | UB25 | USER_LEDS[4] | 114 |
| D15 | UB23 | USER_LEDS[5] | 112 |
| D9 | UB24 | USER_LEDS[6] | 113 |
| D7 | UB22 | USER_LEDS[7] | 106 |





The code to drive the LEDs is either zero (1'b0) or floating (1'bz). First, declare the LED as an output. In the example below, the vector LED is set to 'reg' because it is driven in an always block.



```
//* Module Declaration
module EPT_10CL016_AF_T2_Top (
   input wire
                     CLK 50MHZ,
   input wire
                     RST N,
   //SPI Communications FT-220X
   output wire SPI SCLK,
   input wire
                     SPI MISO,
   inout wire
                     SPI MIOSIO 1,
                     SPI SS,
   output wire
   //User LED Control Registers
   output reg [7:0] USER LEDS,
   //User GPIOs
   input wire [3:0] XIO 1, //XIO -- UB
   //User RGB LED Control Registers
           RGB LED BLUE,
   output reg
   output reg
                     RGB LED RED,
   output reg
                     RGB LED GREEN,
```

To turn the selected LED on, set the signal equal to 1'b0. This will apply a ground to the cathode side of the LED and allow current to flow through the circuit turning the LED on. To turn the selected LED off, set the signal equal to 1'bz. This will float the cathode side of the LED and no current will flow through the LED.



```
//-----
                       _____
// Set the USER LEDS outputs
//-----
always @ (posedge CLK 50MHZ or negedge RST)
begin
 if(!RST)
     USER LEDS <= 8'hz;
 else
 begin
   if (led reset)
     USER LEDS <= 8'hz;
   else if(state[LOAD LEDS])
   begin
     if ( led_reg[0] )
        USER LEDS[0] = 1'b0;
     else
        USER LEDS[0] = 1'bz;
     if ( led_reg[1] )
        USER LEDS[1] = 1'b0;
     else
        USER_LEDS[1] = 1'bz;
     if ( led reg[2] )
        USER LEDS[2] = 1'b0;
     else
        USER LEDS[2] = 1'bz;
     if ( led_reg[3] )
        USER LEDS [3] = 1'b0;
     else
        USER LEDS[3] = 1'bz;
```

3.9 RGB LED

The CycloFlex also includes one RGB LED. It is a SML-LX0404 LED RGB chip. Each LED with the chip is attached to a current limiting resistor. Each LED leg is controlled by a pin from the Cyclone 10 FPGA.





The SML-LX0404 chip is a current sink and are connected to pins on the Cyclone 10. The anode is connected to +3.3V. The series resistors are calculated for current limiting based on +3.3V.





Each series resistor uses a 220 Ohm in a resistor array. The GPIO from the FPGA can be used to control the On/Off of each LED individually. The LED RGB chip uses +3.3V supply and each LED is configured in a Current Sink scheme.

In order to light up the each LED, the user code must assert a zero on the associated signal for the LED. To turn off the LED, assert High Z on the signal.

The LED RGB signals are organized on the following pins from the Cyclone 10 chip:

| LED Number | CycloFlex Schematic Signal | RGB Signal Name | Cyclone 10 Pin Number |
|------------|----------------------------------|-----------------|--------------------------|
| D11 | UB4 | LED_RED | 43 |
| D11 | UB5 | LED_BLUE | 44 |
| D11 | UB6 | LED_GREEN | 49 |

The RGB LED also includes a jumper to turn off the entire chip. This jumper is inline with the +3.3V source to the chip. If the user would like to use the User Bus signals:

- UB4
- UB5
- UB6



For other IO activities, remove the jumper JMP4 and the RGB LED will not light up when the signals are asserted.



3.10 Seven Segment LED Displays

The Seven Segment LED board uses one ACSA02-41SGWA-F01 manufactured by Kingbright. The Display is 0.2 inch digit height. It has low current operation and excellent character appearance. The Super Bright Green source color devices are made with Gallium Phosphide Green Light Emitting Diode.





The GPIOs from the Cyclone 10 are used to control the On/Off of each LED individually. The Seven Segment LED Board is for use only with +3.3V.



Page 47



The ACSA02-41SGWA-F01 chip is a current sink connected to Cyclone 10 IO pins. The anode should be connected to +3.3V. The reason for this is the Series resistors are calculated for current limiting based on +3.3V. Each Segment of the Display is mapped



To a pin on the Cyclone 10 FPGA. When the user would like to form a character on the LED Display, the correct segment must be asserted inside the FPGA.

| LED Display Number | CycloFlex Schematic Signal | Segment Name | Cyclone 10 Pin Number |
|--------------------|----------------------------------|--------------|--------------------------|
| 1 | UB48 | Segment A | 142 |
| 1 | UB30 | Segment B | 141 |
| 1 | UB56 | Segment C | 135 |
| 1 | UB57 | Segment D | 137 |
| 1 | UB31 | Segment E | 136 |
| 1 | UB47 | Segment F | 143 |
| 1 | UB46 | Segment G | 144 |
| 1 | UB55 | Segment DP | 133 |

| LED Display Number | CycloFlex Schematic Signal | Segment Name | Cyclone 10 Pin Number |
|--------------------|----------------------------------|--------------|--------------------------|
| 2 | UB18 | Segment A | 72 |



| 2 | UB17 | Segment B | 71 |
|---|------|------------|-----|
| 2 | UB38 | Segment C | 69 |
| 2 | UB16 | Segment D | 68 |
| 2 | UB15 | Segment E | 67 |
| 2 | UB54 | Segment F | 132 |
| 2 | UB14 | Segment G | 66 |
| 2 | UB39 | Segment DP | 65 |

| LED Display Number | CycloFlex Schematic Signal | Segment Name | Cyclone 10 Pin Number |
|--------------------|----------------------------------|--------------|--------------------------|
| 3 | UB34 | Segment A | 105 |
| 3 | UB35 | Segment B | 100 |
| 3 | UB51 | Segment C | 99 |
| 3 | UB52 | Segment D | 101 |
| 3 | UB53 | Segment E | 103 |
| 3 | UB33 | Segment F | 111 |
| 3 | UB32 | Segment G | 119 |
| 3 | UB50 | Segment DP | 98 |





Each segment of each display uses a current sink method to turn on the segment LED. This means the Anode of each segment LED is connected to the +3.3V (via a Jumper) and the Cathode is connected to the IO of the Cyclone 10. To turn on the Segment LED, the FPGA code must apply a low to the signal.

Page 50



```
always @ (posedge CLK or negedge RST)
begin
  if (!RST)
  begin
      SEVEN_SEGMENT_LED_1 = 8'hz;
      SEVEN_SEGMENT_LED_2 = 8'hz;
      SEVEN_SEGMENT_LED_3 = 8'hz;
  end
  else
  begin
    if (LED DISPLAY ENABLE 1)
    begin
      //LED Display 1 Segment A
      if ( LED DISPLAY BYTE 1[0] )
          SEVEN_SEGMENT_LED_1[0] <= 1'b0;
      else
          SEVEN SEGMENT LED 1[0] <= 1'bz;
      //LED Display 1 Segment B
      if ( LED_DISPLAY_BYTE_1[1] )
          SEVEN_SEGMENT_LED_1[1] <= 1'b0;
      else
          SEVEN SEGMENT LED 1[1] <= 1'bz;
      //LED Display 1 Segment C
      if ( LED DISPLAY BYTE 1[2] )
          SEVEN SEGMENT LED 1[2] <= 1'b0;
      else
          SEVEN_SEGMENT_LED_1[2] <= 1'bz;</pre>
      //LED Display 1 Segment D
      if ( LED_DISPLAY_BYTE_1[3] )
         SEVEN_SEGMENT_LED_1[3] <= 1'b0;
      else
          SEVEN SEGMENT LED 1[3] <= 1'bz;
```

To turn off each segment LED, the FPGA code must apply a tri-state (1'bz) to the signal. In the code section above, the LED Display Byte is received from the Host Software running on the PC (LED_DISPLAY_BYTE_1[7:0]). Each array index represents a segment of the LED Display. The Host PC software and the FPGA code must be aligned with which segment of the Display corresponds to A, B, C, D etc. In the code section above:

• LED_DISPLAY_BYTE_1[0] = LED Display 1 Segment A



- LED_DISPLAY_BYTE_1[1] = LED Display 1 Segment B
- LED_DISPLAY_BYTE_1[2] = LED Display 1 Segment C
- LED_DISPLAY_BYTE_1[3] = LED Display 1 Segment D
- LED_DISPLAY_BYTE_1[4] = LED Display 1 Segment E
- LED_DISPLAY_BYTE_1[5] = LED Display 1 Segment F
- LED_DISPLAY_BYTE_1[6] = LED Display 1 Segment G
- LED_DISPLAY_BYTE_1[7] = LED Display 1 Segment DP

The Seven Segment LED Displays also include a jumpers to turn off each individual display. Each jumper is inline with the +3.3V source to the chip. The following jumpers control the on/off the following:

| LED Display | CycloFlex Schematic Signal | Jumper Schematic Number | J15 Pin Number |
|---------------|----------------------------------|----------------------------|----------------|
| LED Display 1 | A_CC | J15_1 | 1,2 |
| LED Display 2 | B_CC | J15_2 | 3,4 |
| LED Display 3 | C_CC | J15_3 | 5,6 |



Each of the LED segment signals from the Cyclone 10 FPGA are used as IO's on the connectors. If the user would like to use the IO's for other purposes, the jumper selects will turn off the LED Displays. For other IO activities, remove the jumper J15_X jumpers and the associated LED Display will not light up when the segment signals are asserted.

Page 52





3.11 PushButtons

The CycloFlex includes two push button switches. Both are momentary contact switches. They include a 1uF cap to ground to debounce both switches.









| Component | Net Name | Pin Number on Cylcone 10 | Signal in EPT Project Pinout |
|-----------|-------------|-----------------------------|---------------------------------|
| SW1 | PB_SWITCH_1 | 126 | PB_SWITCH1 |
| SW2 | PB_SWITCH_2 | 91 | PB_SWITCH_2 |

Both of these Push Button Switches are configurable as inputs only to the Cyclone 10. The user code can read the state of the switch or use it as an event to trigger some action in the code.





In the above code section, at each rising clock edge of the 50MHz Oscillator the PB_SWITCH_1 and PB_SWITCH_2 are sampled. If either switch are determined low, the "trigger_out' byte assumes the XX_ASSERT byte value.

3.12 Serial Flash

The CycloFlex includes a Serial Flash chip. The chip is P/N: S25FL127SABNFI100Z from Macronix. The S25FL127S device is a flash non-volatile memory product. This device connects to a host system via an SPI. Traditional SPI single bit serial input and output (Single I/O or SIO) is supported as well as optional two bit (Dual I/O or DIO) and four bit (Quad I/O or QIO) serial commands.

All communication between the host system and S25FL-S family of memory devices is in the form of units called commands. All commands begin with an instruction that selects the type of information transfer or device operation to be performed. Commands may also have



an address, instruction modifier, latency period, data transfer to the memory, or data transfer from the memory.

All instruction, address, and data information is transferred serially between the host system and memory device.

All instructions are transferred from host to memory as a single bit serial sequence on the SI signal. Single bit wide commands may provide an address or data sent only on the SI signal. Data may be sent back to the host serially on the SO signal. Dual or Quad Output commands provide an address sent to the memory only on the SI signal. Data will be returned to the host as a sequence of bit pairs on IO0 and IO1 or four bit (nibble) groups on IO0, IO1, IO2, and IO3. Dual or Quad Input/Output (I/O) commands provide an address sent from the host as bit pairs on IO0 and IO1 or, four bit (nibble) groups on IO0, IO1, IO2, and IO3. Data is returned to the host similarly as bit pairs on IO0 and IO1 or, four bit (nibble) groups on IO0, IO1, IO2, and IO3. Commands are structured as follows: • Each command begins with CS# going LOW and ends with CS# returning HIGH. The memory device is selected by the host driving the Chip Select (CS#) signal LOW throughout a command. • The serial clock (SCK) marks the transfer of each bit or group of bits between the host and memory. • Each command begins with an eight bit (byte) instruction. The instruction is always presented only as a single bit serial sequence on the Serial Input (SI) signal with one bit transferred to the memory device on each SCK rising edge. The instruction selects the type of information transfer or device operation to be performed.

• The instruction may be standalone or may be followed by address bits to select a byte location within one of several address spaces in the device. The instruction determines the address space used. The address may be either a 24-bit or a 32-bit address. The address transfers occur on SCK rising edge.

• The width of all transfers following the instruction are determined by the instruction sent. Following transfers may continue to be single bit serial on only the SI or Serial Output (SO) signals, they may be done in two bit groups per (dual) transfer on the IO0 and IO1 signals, or they may be done in 4 bit groups per (quad) transfer on the IO0-IO3 signals. Within the dual or quad groups the least significant bit is on IO0. More significant bits are



placed in significance order on each higher numbered IO signal. Single bits or parallel bit groups are transferred in most to least significant bit order.

• Some instructions send an instruction modifier called mode bits, following the address, to indicate that the next command will be of the same type with an implied, rather than an explicit, instruction. The next command thus does not provide an instruction byte, only a new address and mode bits. This reduces the time needed to send each command when the same command type is repeated in a sequence of commands. The mode bit transfers occur on SCK rising edge.

• The address or mode bits may be followed by write data to be stored in the memory device or by a read latency period before read data is returned to the host. • Write data bit transfers occur on SCK rising edge.

• SCK continues to toggle during any read access latency period. The latency may be zero to several SCK cycles (also referred to as dummy cycles). At the end of the read latency cycles, the first read data bits are driven from the outputs on SCK falling edge at the end of the last read latency cycle. The first read data bits are considered transferred to the host on the following SCK rising edge. Each following transfer occurs on the next SCK rising edge.

• If the command returns read data to the host, the device continues sending data transfers until the host takes the CS# signal HIGH. The CS# signal can be driven HIGH after any transfer in the read data sequence. This will terminate the command.

At the end of a command that does not return data, the host drives the CS# input HIGH. The CS# signal must go HIGH after the eighth bit, of a standalone instruction or, of the last write data byte that is transferred. That is, the CS# signal must be driven HIGH when the number of clock cycles after CS# signal was driven LOW is an exact multiple of eight cycles. If the CS# signal does not go HIGH exactly at the eight SCK cycle boundary of the instruction or write data, the command is rejected and not executed.

• All instruction, address, and mode bits are shifted into the device with the Most Significant bits (MSb) first. The data bits are shifted in and out of the device MSb first. All



data is transferred in byte units with the lowest address byte sent first. Following bytes of data are sent in lowest to highest byte address order i.e. the byte address increments.

• All attempts to read the flash memory array during a program, erase, or a write cycle (embedded operations) are ignored. The embedded operation will continue to execute



without any affect. A very limited set of commands are accepted during an embedded operation. These are discussed in the individual command descriptions.

• Depending on the command, the time for execution varies. A command to read status information from an executing command is available to determine when the command completes execution and whether the command was successful.

| - CS# | |
|----------|-----------------|
| SCK | |
| SI | 7 6 5 4 3 2 1 0 |
| SO - | |
| Phase | Instruction |

Standalone Instruction Command



Single Bit Wide Input Command



Single Bit Wide Output Command

3.12.1 S25FL127S Command Set

Similar to most flash chips, the S25FL127S supports a command set. The user will write a command via SPI protocol and the flash chip will respond.



| Function | Command name | Command description | Instruction value (Hex) | Maximum frequency (MHz) |
|-----------------|--|---|-------------------------|------------------------------------|
| | READ_ID (REMS) | Read Electronic Manufacturer Signature | 90 | 108 |
| Read Device | RDID | Read ID (JEDEC Manufacturer ID and JEDEC CFI) | 9F | 108 |
| identification | RSFDP | Read JEDEC Serial Flash Discoverable Parameters | 5A | 108 |
| | RES | Read Electronic Signature | AB | 50 |
| | RDSR1 | Read Status Register 1 | 05 | 108 |
| | RDSR2 | Read Status Register 2 | 07 | 108 |
| | RDCR | Read Configuration Register 1 | 35 | 108 |
| | WRR | Write Register (Status-1, Configuration-1) | 01 | 108 |
| | WRDI | Write Disable | 04 | 108 |
| | WREN | Write Enable | 06 | 108 |
| | CLSR | Clear Status Register 1 - Erase/Prog. Fail Reset | 30 | 108 |
| | ECCRD | ECC Read (4-byte address) | 18 | 108 |
| Register Access | ABRD | AutoBoot Register Read | 14 | 108 (QUAD=0) 108 (QUAD=1) |
| | ABWR | AutoBoot Register Write | 15 | 108 |
| | BRRD | Bank Register Read | 16 | 108 |
| | BRWR | Bank Register Write | 17 | 108 |
| | Bank Register Access BRAC (Legacy Command formerly used for Deep Power Down) | | В9 | 108 |
| | DLPRD | Data Learning Pattern Read | 41 | 108 |
| | PNVDLR | Program NV Data Learning Register | 43 | 108 |
| | WVDLR | Write Volatile Data Learning Register | 4A | 108 |

3.12.2 Read Identification (RDID 9Fh)



The Read Identification (RDID) command provides read access to manufacturer identification, device identification, and Common Flash Interface (CFI) information. The manufacturer identification is assigned by JEDEC. The CFI structure is defined by JEDEC standard. The device identification and CFI values are assigned by Cypress

The JEDEC Common Flash Interface (CFI) specification defines a device information structure, which allows a vendor-specified software flash management program (driver) to be used for entire families of flash devices. Software support can then be device-independent, JEDEC manufacturer ID independent, forward and backward-compatible for the specified flash device families. System vendors can standardize their flash drivers for long-term software compatibility by using the CFI values to configure a family driver from the CFI information of the device in use.

Any RDID command issued while a program, erase, or write cycle is in progress is ignored and has no effect on execution of the program, erase, or write cycle that is in progress. The RDID instruction is shifted on SI. After the last bit of the RDID instruction is shifted into the device, a byte of manufacturer identification, two bytes of device identification, extended device identification, and CFI information will be shifted sequentially out on SO. As a whole this information is referred to as ID-CFI.

Continued shifting of output beyond the end of the defined ID-CFI address space will provide undefined data. The RDID command sequence is terminated by driving CS# to the logic high state anytime during data output. The maximum clock frequency for the RDID command is 108 MHz.



Read Identification (RDID) Command Sequence



Device ID and Common Flash Interface (ID-CFI) address map

| Byte address | Data | Description |
|--------------|------------------------------|---|
| 00h | 01h | Manufacturer ID for Cypress |
| 01h | 20h (128 Mb) | Device ID Most Significant Byte - |
| | | Memory Interface Type |
| 02h | 18h (128 Mb) | Device ID Least Significant Byte - |
| | | Density |
| 03h | 4Dh | ID-CFI Length - number bytes |
| | | following. Adding this value to the |
| | | current location of 03h gives the |
| | | address of the last valid location in the |
| | | legacy ID-CFI address map. This only |
| | | includes up to the end of the Primary |
| | | Vendor Specific table. The Alternate |
| | | Vendor Specific table contains |
| | | additional information. |
| 04h | 00h (Uniform 256-KB sectors) | Sector Architecture |
| | 01h (4-KB parameter sectors | |
| | with uniform 64-KB sectors) | |
| 05h | 80h (FL-S Family) | Family ID |



| 06h | xxh | Reserved |
|-----|-----|----------|
| 07h | xxh | Reserved |
| 08h | xxh | Reserved |
| 09h | xxh | Reserved |

3.12.3 Register Access commands

Read Status Register 1 (RDSR1 05h)

The Read Status Register 1 (RDSR1) command allows the Status Register 1 contents to be read from SO. The Status Register 1 contents may be read at any time, even while a program, erase, or write operation is in progress. It is possible to read the Status Register 1 continuously by providing multiples of eight clock cycles. The status is updated for each eight cycle read. The maximum clock frequency for the RDSR1 (05h) command is 108 MHz.



Read Status Register 2 (RDSR2 07h)

The Read Status Register (RDSR2) command allows the Status Register 2 contents to be read from SO. The Status Register 2 contents may be read at any time, even while a program, erase, or write operation is in progress. It is possible to read the Status Register 2 continuously by providing multiples of eight clock cycles. The status is updated for each eight cycle read. The maximum clock frequency for the RDSR2 command is 108 MHz.





Read Configuration Register (RDCR 35h)

For the remainder of the access to the registers of the S25FL127S, please see the data sheet.

3.13 Power Input

The CycloFlex is designed to be operated from one of two different power sources:

- Standard USB cable from Laptop/PC.
- +4.5 to +5.5 VDC supplied through the DC power jack. This provides power for a high-efficiency switching regulator on-board to provide +3.3 VDC. The power supply provides reliable power under dynamic loads and high frequency switching internal to the FPGA.

3.14 Communications Interface

The CycloFlex is equipped with a bi-directional communications mechanism. This pathway is via an FT220X USB to SPI bus chip.





The FT220X chip connects the Cyclone 10 FPGA to the Host PC using USB. The FT220X chip provides all of the USB protocol and is transparent to the user. The Input/Output side of the chip provides a modified version of the accepted SPI bus. It uses FTDI's proprietary FT1248 protocol. It has the following features:

- USB to Slave SPI interface in 1-bit mode using the FT1248 protocol
- Data transfer rates to 500 kByte/s
- 512 byte receive buffer and 512 byte transmit buffer utilizing buffer smoothing technology to allow for high data throughput.
- FTDI's royalty-free Virtual Com Port (VCP) and Direct (D2XX) drivers eliminate the requirement for USB driver development.





There are two things that are extremely important to note in the features above:

- SPI interface using the FT1248 protocol
- FTDI's Virtual Com driver

The FT1248 protocol is a deviation from the typical SPI bus scheme. It keeps the SCLK and Chip Select signals typical of SPI. However, it changes the MOSI and MISO application. The FT220X chip changes the MOSI signal to a bi-directional communication port. Earth People Technology has created a Verilog Library to make this change transparent to user code. So, the user is free to create a Master SPI interface within the FPGA code. The second item to note is the FTDI Virtual Com Driver. This driver creates a transparent pathway between the user code in the FPGA and the Host PC. The user can create quite advanced communications schemes very easily with little coding effort.

Earth People Technology has created demonstration software that provides a bi-directional communication pathway that can transfer data at 500Kbytes/second. All source code is provided and the user is encouraged to use this software to as a base to create custom projects for their need.





The USB-C connector provides a path between the Host PC and the CycloFlex Board. It provides a transparent means to power the board and bi-directional communications. The communications occurs over USB. The FTDI driver provides a convient transparent pathway to the CycloFlex Board. The user code in the FPGA is only required to meet the requirements of the FT220X chip.

| Component | Function | Net Name | Pin | Signal in EPT Project |
|-----------|----------|----------|------------|-----------------------|
| | | | Number on | |
| | | | Cylcone 10 | |
| U1 | MIOSIO0 | UB27 | 120 | SPI_MIOSIO_1 |
| U1 | MISO | UB26 | 115 | SPI_MISO |
| U1 | SCLK | UB29 | 125 | SPI_SCLK |
| U1 | SS | UB28 | 121 | SPI_SS |

The FT220X chip is located in the upper left corner of the CycloFlex board. It has four connections to the FPGA.





The FT220X chip DOES NOT use the typical SPI bus protocol. It uses a modified protocol, the FT1248. The difference between normal SPI and the FT1248 protocol is the MOSI data line is NOT a single direction data line. The FT1248 protocol makes this line a bi-direction data line. For data transmitted from the FPGA to the FT220X, the host (FPGA user code) must send a command via the MOSI line then read back the data from the MOSI line. The FT220X renames the MOSI line to the MIOSIO[x] signal. "x" Because the chip has four of these IO lines available to increase bandwidth. Here is the timing diagram for the FT220X basic Read/Write cycle.





During the Read Cycle, the Host (FPGA user code) sends a command to the FT220X, then reads the data bytes from the chip. All via the MIOSIO[0] signal.

During the Write Cycle, the Host (FPGA user code) sends a command to the FT220X, then transmits the number of bytes to the chip. All via the MIOSIO[0] signal.

| Command | Identifier | Description |
|--------------------|------------|---|
| | | |
| Write | 0x00 | Write request command |
| Read | 0x01 | Read request command |
| Read modem status | 0x02 | Read modem status command, users |
| | | may wish to emulate modem status |
| | | control. A RMS command returns |
| | | status bits RTS and DTR |
| Write modem status | 0x03 | Write modem status command, users |
| | | may wish to emulate modem status |
| | | control. A WMS command allows |
| | | users to set status bits: DCD, RI, DSR, |
| | | CTS |

The commands that the Host must send to the FT220X chip are:



| Write buffer fluch | 004 | Write huffer fluch request This |
|--------------------|------------|--|
| write buller hush | 0X04 | write buller flush request – This |
| | | command is used to indicate to the |
| | | FT1248 slave that its write buffers |
| | | should be flushed rather than wait for |
| | | any latency timers to expire. If this |
| | | command is received the FT1248 |
| | | block will flag the upstream |
| | | controllers (USB FIFOs etc) to flush |
| | | their write buffers regardless of what |
| | | content is present in the FT1248 write |
| | | buffer |
| Address eeprom | 0x05 | Address EEPROM command sets the |
| | | address users wish to write or read |
| | | from |
| Write eeprom | 0x06 | Write EEPROM command sets the |
| | | write data to be written into the |
| | | EEPROM |
| Read eeprom | 0x07 | Read EEPROM command reads |
| Read USB status | 0x08 | Read USB Status: |
| | | 00 = suspended, $01 =$ default, $10 =$ |
| | | addressed, $11 = \text{configured}$ |
| Reserved | 0x09 - 0xF | Unused Commands |

3.14.1 CONNECT LED

The CycloFlex has a "CONNECT" LED installed on the board. If the USB Driver is installed properly on the Host PC (See the Load EPT Drivers Section), once the USB cable is connected to the USB-C connector, this LED will light up.





The purpose of this LED is to inform the user that the following has occurred:

- USB Driver is properly installed on the Host PC
- The USB-C cable is properly installed
- The +3.3V power supply is functioning properly
- The FT220X is functioning properly

These four items will provide reasonable assurance that the USB section of the CycloFlex is functioning properly. The user can further use the pre-installed FPGA project to ensure that other parts of the CycloFlex board are functioning properly. See the section "Getting Started with the CycloFlex" for the use of the pre-installed FPGA project and its capabilities.

3.14.2 Active Host Communications

Earth People Technology has developed a robust software SDK that allows the user to easily create a bi-directional communications scheme with minimal coding effort.




3.14.3 CONF DONE LED

The CONF_DONE LED is connected directly to the FPGA CONF_DONE signal.



When this LED is lit, it signals to the user that the FPGA has been correctly configured from the configuration flash or the JTAG connection.





The purpose of this LED is to inform the user that the following has occurred:

- Power to the CycloFlex has been successful
- The +3.3V, +2.5V and +1.2V power supplies are functioning properly
- The Cyclone 10 chip is functioning properly
- The Cyclone 10 chip has been properly programmed with a valid FPGA project

These four items will provide reasonable assurance that the power and programming section of the CycloFlex is functioning properly. The user can further use the pre-installed FPGA project to ensure that other parts of the CycloFlex board are functioning properly. See the section "Getting Started with the CycloFlex" for the use of the pre-installed FPGA project and its capabilities.

3.15 JTAG Interface

The CycloFlex has a 5x2 header for use in programming the Cyclone 10 FPGA via JTAG. The connector is located in the bottom right corner of the CycloFlex. It is shrouded and keyed to allow easier insertion.





This connector uses the standard Altera Blaster connector pinout.



The VCC(TRGT) is set to +3.3V on the CycloFlex. This voltage is used to set the output voltage I/O level on the Altera Blaster. For the CycloFlex, +3.3V is the I/O level required. The board is 100% compatible with all Altera Blasters. The board requires power from either Barrel Connector or USB-C Connector. Then connect the Blaster.





The CycloFlex includes programming switch that capable of six Dual Pole Single Throw connections. The JTAG/CONFIG SWITCH.



This switch is designed to allow the external Blaster Programmer to either program the Cyclone 10 chip directly using JTAG or program the Config Flash chip. Changing the position of the switch will allow the same Blaster to be used for either JTAG programming or Config Flash programming.

Page 76





The JTAG Programming Path must have certain configuration pins of the Cyclone 10 in fixed positions (pulled up or pulled down) during programming. The following jumpers must be installed for correct programming of the Cyclone 10 chip using JTAG:

- JMP7
- JMP6
- JMP5

A jumper is a two pin socket used to short two header pins together.







The jumper locations are:





The correct settings for JTAG Path Programming:





Once the jumpers and JTAG/Flash switch have been set, refer the section "Programming the CycloFlex" for instructions on how to use the Quartus Prime Lite software to program the Cyclone 10 chip.

3.16 Configuration Flash Programming

The Configuration Flash is used to store the users synthesized object file for use when the power to the CycloFlex board is cycled (on/off).





The CycloFlex uses the same 10 pin connector for Configuring the Flash chip with the following pinout:



The board requires power from either Barrel Connector or USB-C Connector. Then connect the Blaster.

Page 81





The CycloFlex includes programming switch that capable of six Dual Pole Single Throw connections. The JTAG/CONFIG SWITCH.



This switch is designed to allow the external Blaster Programmer to either program the Cyclone 10 chip directly using JTAG or program the Config Flash chip. Changing the position of the switch will allow the same Blaster to be used for either JTAG programming or Config Flash programming.

Page 82





The JTAG Programming Path must have certain configuration pins of the Cyclone 10 in fixed positions (pulled up or pulled down) during programming. The following jumpers must be installed for correct programming of the Configuration Flash:

- JMP7
- JMP6
- JMP5

A jumper is a two pin socket used to short two header pins together.







The jumper locations are:





The CycloFlex should be configure with the following:





Once the jumpers and JTAG/Flash switch have been set, refer the section "Programming the CycloFlex" for instructions on how to use the Quartus Prime Lite software to program the Cyclone 10 chip.

4 Powering the CycloFlex

There are a few options for powering the CycloFlex Board. You can run the CycloFlex from a laptop with 2.5W of power. Or you can run it from the +5V @ 2A wall USB chargers for 10W of power. The barrel connector can handle up to +5.5V @ 3 A for 15W of power.

- Standard USB cable from Laptop/PC.
- +5 VDC wall charger (phone charger) through USB cable.
- +4.5 to +5.5 VDC supplied through the DC power jack.





The barrel connector is the typical size used on many popular DIY boards such as the Arduino series. It has the following mechanical specs:

- 2.0mm Inner Diameter
- 5.5mm Outer Diameter

The barrel connector does not include a diode protection to prevent reverse polarity connection. So, care must be exercised when connecting up your cable to the barrel connector. Please ensure the correct polarity connections are made before connecting to the CycloFlex. Also, there is no discrete protection to the power input. The power supply does include a high current protection circuit. The current limit is around 4.7Amps. But, the CycloFlex is only designed to handle 2Amps of current. So, damage may occur to the CycloFlex if the user does not exercise care in design and use of the Inputs/Outputs.





Power the CycloFlex directly from the PC. +5V@0.5A



Power the CycloFlex directly from the wall charger. +5V~6V@2A

5 EPT Drivers

The CycloFlex Development system requires drivers for any interaction between PC and the board. The communication between the two consists of programming the FPGA and data

Page 88



transfer. In both cases, the USB Driver is required. This will allow Windows to recognize the USB Chip and setup a pathway for Windows to communicate with the USB hardware.

5.1 USB Driver

The CycloFlex uses an FTDI FT220X USB to Slave SPI chip. This chip provides the USB interface to the PC and the serial/FIFO interface to the FPGA. The FT220X requires the use of the FTDI USB driver. To install the driver onto your PC, use the EPT_Serial_Driver Folder. The installation of the FTDI 2.12.xx driver is easily accomplished by double clicking the CDM212xx_Setup.exe.

Locate the EPT_Serial_Driver folder in the Drivers folder of the CycloFlex_USB_FPGA_PROJECT_x.x_DVD using Windows Explorer.





| 📙 🔄 📜 🗢 C:\Jolly\Products\Earth Peo | ple Technology\DUEPROLOGIC_USB_ | FPGA_PROJECT_4.0_DVD\D | rivers\EPT_Seri | | | |
|--|---|-------------------------|----------------------|---|---------------------|-------------------------------------|
| File Home Share View Image: Share Image: Share Image: Share Image: Share Image: Share Pin to Quick Copy Paste Image: Share Image: Share Image: Share Pin to Quick Copy Paste Image: Share Image: Share | Move Copy to' to' Organize | New item • | Properties | Select all Select none Invert selection Select | | |
| ← → × ↑ 🖡 → This PC → Windows | (C:) > Jolly > Products > Earth I | People Technology → DUE | PROLOGIC_USB_FPGA_PR | OJECT_4.0_DVD → Drivers | > EPT_Serial_Driver | ✓ Ŏ |
| Earth People Technology Sol. 100M, DEV_SYS_PROJECT. DUEPROLOGIC_USB_FPGA_PRC DUEPROLOGIC_USB_FPGA_PRC Documentation Documentation Dorivers EPT_JTAG_Blaster EPT_Senia_Driver | 2.8_DVD UECT_3.0_DVD UECT_4.0_DVD | Name CDM21228_St | etup.exe | ~ | | Date modified 3/29/2021 10:15 AM |
| Projects_ActiveHost Projects_Arduino Projects_HDL Projects_HDL FT_4CE6_AF_Data_Collecto EPT_4CE6_AF_Platform_Dem | r 0 | v < | | | | |

Double click on the *.exe file and select the default settings when the software tool queries the user.

Plug in the CycloFlex into an available USB port.



Windows will attempt to locate a driver for the USB device. Allow Windows to install the driver for the CycloFlex.

If Windows cannot load a driver for the CycloFlex, a notification window will inform the user that the driver load has failed for the device.

Page 90



| | . ₹ Manage | 1 | b/\ | | | | _ | | × |
|---------|--------------------------------------|-----|-----|---------------------------------------|---|-----------------------|------------|-------------|------|
| File | Device Manager | | | | | - □ > | | | × |
| > -> | File Action View Help | | | | | | P Sea | ch DVD RW | Driv |
| The Lib | ♦ ♥ □ 0 0 9 | | | | | | s | ize | |
| E C | V DESKTOP-H1MP0LM | | _ | | | | ~ | | |
| D | > Audio inputs and outputs | | | | | | | | |
| b N | > @ Cameras | | | | | | | | |
| | > 🛄 Computer | | | | | | sett | 1 KB | |
| Pi Pi | > Disk drives | | | | | | | | |
| 📃 Si | > 🕞 Display adapters | | | | | | | | |
| I Vi | > DVD/CD-ROM drives | | | | | | | | |
| O DV | > IDE ATA/ATAPI controllers | | | | | | | | |
| | > Jungo Connectivity | | | | | | | | |
| * | > 🛄 Keyboards | | | | | | | | |
| Net | > () Mice and other pointing devices | 8 | | | | | | | |
| ems | > 🥅 Monitors | | | | | | | | |
| | > 🗇 Network adapters | | | | | | - | | X |
| | ✓ M ^D Other devices | | | | | | | | |
| He | FT220X 4-BIT FT1248 | | | | | | | | ~ |
| | Airoha_App | | | | | | Search | Earth Peop | le |
| | > Print queuer | | | | | | | | |
| | > Printers | | | | | | | Type | |
| F | > Processors | | | | | | - IVI | File Tolde | 1 |
| | > Security devices | | | | | | M | File folde | r i |
| | > Software devices | | | | | | -M | File folde | 5 |
| M | > 🖏 Sound, video and game controll | ers | | | | | м | File folder | £. |
| M | > 🎥 Storage controllers | | | | | | M | File folder | t |
| Or | Sustem devices | | | | | | M | File folder | 1 |
| PE | VIICIO | - | _ | | _ | | M | File folde | 5 |
| Pe | fLoos | | | UNO_SERIAL_GRAPH_TOOL_PROJECT_1.5_CD | | | | | 3 |
| - | Server Files | | | UNOMAX_CPLD_SYSTEM_PROJECT_2.7_DVD | 0 | Setting up a device | 2.27 | | 8 |
| Pro | igram rites | | | UNOPROLOGIC2_USB_CPLD_PROJECT_2.6_DVD | | We're setting up 'USB | <-> Serial | | |
| Pro | gram Files (x86) | ~ | 1 | | | Converter'. | | | |

Right click on the "FT220X 4-BIT FT1248" icon that failed to load. Then select the "Load driver from Known Location". Navigate to the

CYCLOFLEX_USB_FPGA_PROJECT_x.x_DVD/drivers/EPT_Serial_Driver folder. Allow the Windows PC to locate and install the driver.

If this method continues to fail, contact support at Earth People Technology using the following methods:

www.earthpeopletechnology.com/Forums support@earthpeopletechnology.com sales@earthpeopletechnology.com

If the driver is successfully installed, Windows will inform the user. The user can check Device Manager to ensure the correct driver was installed for the CycloFlex. The CycloFlex will show up as two COM Ports under the "Ports (COM &LPT)" under the Device Manager.



| 占 De | evice Manager |
|-------------|---------------------------------|
| File | Action View Help |
| <pre></pre> | |
| > | Biometric devices |
| > | 8 Bluetooth |
| > | Q Cameras |
| > | Computer |
| > | Disk drives |
| > | 🕎 Display adapters |
| > | 📔 Firmware |
| > | 🛺 Human Interface Devices |
| > | 🔤 Keyboards |
| > | Memory technology devices |
| > | Mice and other pointing devices |
| > | Monitors |
| > | 🚽 Network adapters |
| > | 2 Other devices |
| ~ | Ports (COM & LPT) |
| | 💭 USB Serial Port (COM3) |
| > | 📼 Print queues |
| > | Printers |
| > | Processors |
| > | P Security devices |
| > | E Sensors |

When this is complete, the drivers are installed and the CycloFlex can be used for programming and USB data transfers.

6 Installing Quartus

You must install Quartus Prime to configure the CycloFlex. Altera Quartus Prime must be downloaded from the Altera website.

Download the Quartus Prime by following the directions in the Section Downloading Quartus.

6.1.1 Downloading Quartus

The first thing to do in order build a project in Quartus is to download and install the application. You can find the latest version of Quartus at:

Intel FPGA Quartus Prime Lite



Please be advised, Intel is prone to changing their website graphics every few months. The guide below is several months out of date. Please follow the latest instructions on the Quartus Prime Lite Download website. The instructions here are only meant as a guide to getting the software downloaded.

You will first need to apply for an account with Intel. Then use your login and password to access the download site. Click on the Download Windows Version.

| intel. PROF | DUCTS SUPPORT | SOLUTIONS DEVE | LOPERS PARTNERS | FOUNDRY | | | Q Search Intel.com |
|------------------|---|--|--|---|---|---|---|
| FPGA Software Do | wnload Center 🗸 | | | | | | |
| | Intel [®] Wind | Quartus® ows | Prime Lite E | dition Design S | Software Vers | ion 22.1 fc | or |
| | ID | Date | Software Type | Software Package | Version | Operating Sy | stems |
| | 757262 | 11/4/2022 | FPGA Development | t 👻 Quartus® Prime Lite | ✓ 22.1 | ✓ Windows | ✓ |
| Freehook | The Intel® Qu and follow th Users should Intel® Quartu a newer vers subscribe to If you are usi version 22.1, To find softw • Refer to t • User the | uartus [®] Prime Lite Editio le technical recommend l promptly install the la s [®] Prime Lite Edition Dr our customer notificati ng floating license serv doesn't work with old vare versions that suppor to Everice Support List oftware Selector | on Design Software, Version Dations to help improve sect lest version upon release. esign Software, Version 22.1 orted by this version are obso n mailing list. er for Intel FPGA software, y version of daemon software ort specific device families: | 22.1 includes functional and securit urity. Additional security updates are is subject to removal from the web solete. If you would like to receive cu rou need to upgrade to the latest lice . You can download the daemon soft | y updates. Users should keep planned and will be provided when support for all devices i stomer notifications by e-mai ense daemon software (v11.18 tware from this link | their software up-to- las they become ava n this release are ava l, please subscribe to 3.2.0). Intel FPGA soft | -date Ilable. ilable in our ware, |

Scroll down the page to the "Downloads" section.



Feedback

| Knowle Probler Dow Mult | Issues and Patche dge Base: Search ns and Answers of NIOADS | is for the Intel® Quar for Errata. n specific IP or Produ Individual Files | Additional Software | Copyleft Lice | insed Source | | |
|--|--|--|---|--|--|---|----------------|
| Multir | ole Download | | | | | | |
| Inte | el® Quartus® Prin | ne Lite Edition Sof | ftware (Device support | included) | | | |
| | | Download | | Size: 5.5 GB | | | ~ |
| | Quartus | -ute-22.13td.0.515-4 | windows.tai | | | | |
| | | dows requires obuit | ntu 18.04 LIS on Window | s Subsystem for l | inux (WSL), which requi | res a manual installatio | n. |
| ** N ** To What | ios® II EDS require otal space require at's Included? | d is 26.10 GB includi | itu 18.04 LI S on Window clipse IDE manually. ing tar file (5.48 GB), unta | s Subsystem for l rred files (5.48 GE | inux (WSL), which requi | res a manual installatio GB) | n. |
| ** N ** Ti What Downle 1. Dow 2. Extr 3. Run | ios [®] II EDS require otal space required at's Included? mload the softwar act the files into the the setup.bat file. | sy ou to install an Ec d is 26.10 GB includi structions: re tar file and the ap | Itu 18.04 LIS on Window clipse IDE manually. ing tar file (5.48 GB), unta ppropriate device support directory. | s Subsystem for l rred files (5.48 GE ; files. | inux (WSL), which requi | res a manual installatio . GB) | n. |
| ** N ** Tr What 1. Dow 2. Extr 3. Run Read In | ios [®] II EDS require otal space required at's Included? and and install ins molad the softwar act the files into the the setup.bat file, tel [®] FPGA Softwar | syou to install an Ec d is 26.10 GB includi structions: re tar file and the ap he same temporary of re Installation FAQ | tu 18.04 LIS on Window clipse IDE manually. ing tar file (5.48 GB), unta ppropriate device support directory. | s Subsystem for l rred files (5.48 GE ; files. | inux (WSL), which requi | res a manual installatio | n. |
| ** N ** Ti Wh Downld 1. Dow 2. Extr 3. Run Read In Note: T | ios [®] II EDS require otal space required at's included? and and install insymbol miload the softwar act the files into the the setup.bat file, tel® FPGA Softwar he Intel® Quartus® | syou to install an Ec d is 26.10 GB includi structions: re tar file and the ap ne same temporary of re Installation FAQ Prime software is a | Itu 18.04 LIS on Window clipse IDE manually. ing tar file (5.48 GB), unta opropriate device support directory. | s Subsystem for l rred files (5.48 Gf files. ct. Depending on | inux (WSL), which requi) and installation (15.13 your download speed, d | res a manual installatio GB) ownload times may be | n. |
| ** N ** T Wh Downlo 1. Dow 2. Extr 3. Run Read In Note: T Detai | ios® II EDS require tat space require at's Included? And and install ins unload the softwar act the files into it the setup.bat file. FPGA Softwar he Intel® Quartus® led Descriptic | sy out of install an Ec d is 26.10 GB includi structions: re tar file and the ap he same temporary of re Installation FAQ Prime software is a ON | Itu 18.04 LTS on Window clipse IDE manually. ing tar file (5.48 GB), unta opropriate device support directory. full-featured EDA produ | s Subsystem for l rred files (5.48 GF files. :t. Depending on | inux (WSL), which requi | res a manual installatio . GB) ownload times may be | n. lengthy. |
| ** N ** Ti Wh: 1. Dow 2. Extr 3. Run Read In Note: T Detai System | ios [®] II EDS require tat space require at's Include? oad and install ins unload the softwar act the files into ti the setup.bat file. tel [®] FPGA Softwar he Intel [®] Quartus [®] led Descriptic Requirements: | sy out of install an EC of sy out of install an EC of structions: re tar file and the ap ne same temporary of re Installation FAQ Prime software is a on | Itu 18.04 LTS on Window clipse IDE manually. ing tar file (5.48 GB), unta opropriate device support directory. full-featured EDA produ | s Subsystem for l rred files (5.48 Gf files. ct. Depending on | inux (WSL), which requi | res a manual installatio . GB) ownload times may be | n. lengthy. |
| ** N ** Ti Wh Downle 1. Dow 2. Extr 3. Run Read In Note: T Detai System Operati | ios ^a II EDS require tal space requires at's Include? and and install in mload the software act the files into ti the setup.bat file. tel ¹² PPGA Softwar he Intel ⁴ Quartus ⁴ led Descriptic Requirements: ng System Suppo | sy out of install an EC de you to install an EC de is 26.10 GB includi structions: re Lar file and the ap he same temporary (e Installation FAQ Prime software is a con | Itu 18.04 LTS on Window clipse IDE manually. ing tar file (5.48 GB), unta oppropriate device support directory. | s Subsystem for I rred files (5.48 Gf : files. :t. Depending on | inux (WSL), which requi | res a manual installatio GB) ownload times may be | n. lengthy. |

Click on the "Download Quartus-lite-22.1 xxxxxx Windows Tar.



| Critical Issues and Patches for the Intel® Quartus® Prime Lite Edition Software, Version 22.1. Knowledge Base: Search for Errata. Problems and Answers on specific IP or Products. |
|--|
| Downloads |
| Multiple Download Individual Files Additional Software Copyleft Licensed Source |
| Multiple Download |
| Intel® Quartus® Prime Lite Edition Software (Device support included) Download Quartus=lite=22,1std.0.915-windows.tar ** Nios® II EDS on Windows requires Ubuntu 18.04 L1S on Windows Subsystem for Linux (WSL), which requires a manual installation. ** Nios® II EDS equires you to install an Eclipse IDE manually. ** Total space required is 26.10 GB including tar file (5.48 GB), untarred files (5.48 GB) and installation (15.13 GB) What's Included? |
| Download and install instructions: 1. Download the software .tar file and the appropriate device support files. 2. Extract the files into the same temporary directory. 3. Run the setup.bat file. Read Intel® FPGA Software Installation FAQ |
| Note: The Intel [®] Quartus [®] Prime software is a full-featured EDA product. Depending on your download speed, download times may be lengthy. |
| Detailed Description System Requirements: Operating System Support |
| Minimum Disk Space for Intel® FPGA Software |
| through the Legal Stuff. |



| | T 175' 1' |
|--|--|
| | Legal Disclaimer |
| PLEASE N and security term, which Intel® FPG. Quartus® Pr Builder for I | OTE: This version of software ("Software") does not contain the latest functional updates. In order to use this version, you must first acknowledge the following supplements and supersedes any inconsistent provision in the version of the A Software License Subscription Agreement for the product (e.g., Intel® time Software, Intel® HLS Compiler, Intel® FPGA SDK for OpenCL TM , DSP ntel® FPGAs, or Advanced Link Analyzer) with which you use the Software: |
| Intel does no | t give or enter into any condition, warranty, or other term: |
| i. with r infect | espect to any malfunctions or other errors in its Software caused by virus, ion, worm or similar malicious code not developed or introduced by Intel; or |
| 11. to the | effect that any Software will protect against all possible security threats, |
| servio | e interruption for any lost or stolen data or systems or for any other damages |
| arisin | g out of or relating to any such actions or intrusions or resulting from use of |
| Softw | are. Intel does not give or enter into any condition, warranty, or other term with |
| respe | t to interoperability. |
| Intel does no | ot warrant or assume responsibility for the accuracy or completeness of any |
| information | text, graphics, links or other items within the Software. Please click "Accept" |
| below to con | tinue the download process. |
| | Accept |

This will start the download.



| | | | | | | | | | | | | | - | | |
|-------------|-------|---------|-------------------|------------|--------------|-----------|----------------|-------------|-------------|-----------|----------|----------|-------|------------|-----|
| | | | Quartus-lite-22.1 | | | | | | | | | | \$ | ۰ (8 | |
| Google Maps | 🗅 EPT | 🗀 Banks | Electronics | 🗅 News | 🗀 Music | 🗀 Pay | 🗀 Markets | C Reference | 🗀 Knowledge | 🗅 Tickets | 🗀 Nights | | » I Z |] All Bool | cma |
| | | | | | | | | | | | | | / | | |
| | (| intel | Software Li | cense Agr | eement | | | | | | | / | | | |
| | | Th | ank you. You | ır docume | nt should | downlo | ad automat | tically. | c | HECK TI | HE DOW | NLOAD PI | ROGE | RESS | |
| | | I | f the file does | not start | to downlo | ad, plea | se click thi | s link | | | | | | | |
| | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | |
| | | Ter | ms of Use Pr | ivacy Le | gal Informat | ion ©] | Intel Corporat | tion | | | | | | | |
| | | | | | | | | | | | | | | | |

The file is 13.9 GB (or greater), so this could take a couple of hours depending on your internet connection. When download is complete, store the *.tar file in a directory on your PC.



| 📙 🕑 📑 🖛 C:\Jolly\Downloads\Altera_Intel_FPGA\Quartus Prime 20.1 | | |
|---|---------------------------------------|-----------------|
| File Home Share View | | |
| ← → → ↑ 🔒 > This PC > Local Disk (C:) > Jolly > Downloads > A | ltera_Intel_FPGA → Quartus Prir | ne 20.1 |
| Code_FPGA | ^ Name | ^ Date modified |
| | | |
| Downloads | | In |
| 🔒 Allegro | | |
| Altera_Intel_FPGA | | |
| 📙 Quartus Prime 16 | · · · · · · · · · · · · · · · · · · · | |
| Quartus Prime 17.1 | | |
| Quartus Prime 18.1 | | |
| Quartus Prime 20.1 | | |
| AtmosFX | | |
| Camtasia | | |
| FTDI | | |
| HyperSerialPort | | |
| 🖊 🎚 🛃 🚽 🛛 C:\Users\nelso\Downloads | | |
| File Home Share View | | |
| ← → ~ ↑ 🕂 → This PC → Local Disk (C:) → Users → nelso → Downloa | ds | |
| 💻 This PC | ^ Name | |
| 🧊 3D Objects | ✓ Today (1) | |
| 📃 Desktop | Quartus-lite-20.1.0.7 | 11-windows.tar |
| Documents | Earlier this week (1 | |
| 🕂 Downloads | A Label-501986027.pdf | |
| 👌 Music | V last week (1) | |
| Pictures | Label-501432708 pdf | |
| Videos | Last month (10) | |
| 🏪 Local Disk (C:) | V Last month (18) | |

Use a tool such as WinZip to Extract the *.tar file.



| 💐 💾 💕 🖡 🔻 Quartus-lite | e-20.1.0.711-win | dows - WinZip Evaluat | tion Version - 21 day | ys left | | – 🗆 X |
|--|------------------|---------------------------------|--|--|--|-------------------------------|
| File Unzip/Share Edit | Backup T | ools Settings | View Help | Buy Now | | ~ () |
| | D BUY | NOW Activate Wi Purchase ris | inZip before your tria sk-free TODAY from o | I runs out! our secure online shop. | Cnet, CNET editors rating | |
| Files * + < Files | > Qua | artus-lite-2 | 20.1.0.711 | -windows.t | tar | Actions > Unzip All Files |
| Recent Zip Files Quartus-lite-20.1.0.7tar Quartus Prime 20.1 | | components Type: Folder | | Date mod | lified: 6/6/2020 6:33 PM | Unzip to: ~\Quartus-lite-20.1 |
| Browse & Manage Files | | readme.txt Type: Readme Docu | ment | Date moo Size: 8.51 | dified: 6/6/2020 7:09 PM KB → 8.51 KB | Convert & Protect Files |
| Frequent Folders | | setup.bat Type: Windows Batc | h File | Date mod Size: 1.07 | lified: 6/6/2020 7:09 PM KB → 1.07 KB | Encrypt Off |
| This PC 648 GB free of 930 GB | | | | | | Reduce Photos Off |
| Network | | | | | | Remove Info Off |
| Shared Files | | | | | | Convert to PDF Off |
| Add Cloud | | | | | | Combine PDFs Off |
| | 3 ite | m(s) | | | Zip File: 11 item(s), 5.90 GB | Save or Share Zip |

The tool will unpack all files.

| WinZip | | | × |
|--|-----------|----------|---|
| Extracting ModelSimSetup-20.1.0.711-wi | ndows ex | - | |
| Exclusion of the second s | indows.ex | - | |
| | | | |
| | | | |
| Cancel | | | |

6.1.2 Quartus Installer

When the unpacking finishes from the previous section, double click the setup.bat file in the download folder.



| 📙 🛃 📙 = C:\Jolly\Downloads\Altera_In | itel_FPGA\Quartus Prime 20.1 | | | | |
|--|---------------------------------|--------------------------|-------------------------|---|--------------------|
| File Home Share View | | | | | |
| Pin to Quick access Copy Paste Copy path Paste shortcut Paste shortcut | Move Copy to * Copy | New item • | Properties ▼ History | Select all Select none Invert selection | |
| Clipboard | Organize | New | Open | Select | |
| ← → × ↑ 📙 > This PC → Local Disk | (C:) > Jolly > Downloads > Alte | era_Intel_FPGA → Quartus | Prime 20.1 | | |
| Quartus Prime 16 | | ^ Name | ^ | Date modified | Туре |
| Quartus Prime 17.1 | | components | | 8/8/2020 12:58 PM | File folder |
| Quartus Prime 18.1 | | 🔍 Quartus-lite-20 | .1.0.711-windows.tar | 8/8/2020 12:25 PM | WinZip File |
| > 📙 Quartus Prime 20.1 | | readme.txt | _ | 6/6/2020 7:09 PM | Text Document |
| > AtmosFX | | 💿 setup.bat | | 6/6/2020 7:09 PM | Windows Batch File |
| > 🔤 Camtasia | | | | | |
| > 📙 FTDI | | | | | |
| > 📙 HyperSerialPort | | | | | |

Click "Next" on the Introduction Window.



| 🕞 Installing Quartus Prime Lite Edition (Free) 20.1.0.711 | | | | × |
|---|---|--|--|-------------------------|
| | Setup - Quartus Prime Lite Edition (Free) 20.1.0.711 | | | |
| intel | Welcome to the Quartus Prime Lite Edition (Free) 20.1.0.711 Setup Wizard. The Quartus Prime software requires that your system have sufficient physic targeting specific devices. You can check the "Memory Recommendations" set Software and Device Support Release Notes" (https://www.intel.com/content/www/us/en/programmable/documentation/lit memory requirements for a particular device. For more information about Intel FPGA software, go to https://www.intel.com/content/www/us/en/products/programmable.html. | al RAM to ction in th t-rn.html) | compile d e "Quartu: for detaile | esigns s Prime ed |
| | | | | |
| | < Back Ne | ext > | Can | cel |

Click the checkbox to agree to the license terms. Then click "Next".



| 🕞 Installing Quartus Prime L | ite Edition (Free) 20.1.0.711 | | - | | × |
|--|--|--|--------------------------------|----------|-----|
| License Agreement | | | | (inl | tel |
| You can view the full license ag files before the installation. Yo http://fpgasoftware.intel.com | greement at the link below or useinstall_lic u must accept the terms of the agreement be <u>/eula/</u> | option from command-line to g efore continuing with the insta | get the license a allation. | agreemen | t |
| QUARTUS PRIME AND IN Intel, Quartus and the In or its subsidiaries in the trademarks and trade na respective owners. | TEL FPGA IP LICENSE AGREEMENT, V tel logos are trademarks of Intel Corp US and other countries. Any other times referenced here are the propert | ERSION 20.1 oration y of their | | | ^ |
| DO NOT DOWNLOAD, IN LICENSED SOFTWARE U CONDITIONS OF THIS A | STALL, ACCESS, COPY, OR USE ANY F NTIL YOU HAVE READ AND ACCEPTED GREEMENT. BY INSTALLING, COPYING, | ORTION OF THE THE TERMS AND ACCESSING, OR | | | ~ |
| < | | | | > | |
| Do you accept this license? | I accept the agreement I do not accept the agreement | | | | |
| InstallBuilder | | < Back | Next > | Cano | cel |

Click "Next" and accept the defaults.

At the Select Products Window, de-select the Quartus Prime Supbscription Edition by clicking on its check box so that the box is not checked. Then click on the check box by the Quartus Prime Web Edition (Free).



| 🕞 Installing Quartus Prime Lite Edition (Free) 20.1.0.711 | - | |
|--|---|---------|
| Select Components | | (intel) |
| Select the components you want to install | | |
| Quartus Prime Lite Edition (Free) Quartus Prime (includes Nios II EDS) (9313MB) Quartus Prime Help (508.4MB) Devices Arria II (536.5MB) Cyclone IV (516.3MB) Cyclone IV (16.3MB) Cyclone V (1434.3MB) MAX II/V (13.1MB) MAX 10 FPGA (360.3MB) ModelSim - Intel FPGA Edition (Free) (4318.8MB) ModelSim - Intel FPGA Edition (4318.8MB) | Installs Arria II device support. (536.5MB) | |
| InstallBuilder | < Back Next > | Cancel |

Click "Next" to accept the defaults



| 🕞 Installing Quartus Prime Lite Edition (Free) 20.1.0.711 | — | | × |
|--|--------|--------|---|
| Ready to Install | | (inte | D |
| Summary: Installation directory: C:\intelFPGA_lite\20.1 Required disk space: 16760 MB Available disk space: 657864 MB | | | |
| InstallBuilder Sack 1 | Vext > | Cancel | I |

Click "Next" to accept the defaults



| 📚 Installing Quartus Prime Lite Edition (Free) 20.1.0.711 | | - | | × |
|---|--------|--------|------|----|
| Installing | | | (int | el |
| Wait while Setup installs Quartus Prime Lite Edition (Free) 20.1.0.711 Installing Unpacking files | | | | |
| | | | | |
| | | | | |
| | | | | |
| | | | | |
| | | | | |
| | | | | |
| | | | | |
| InstallBuilder | | | | |
| | < Back | Next > | Cano | el |

Wait for the installation to complete.







| 🕤 Installing Quartus Prime I | ite Edition (Free) 20.1.0.711 | - | | × |
|------------------------------|---|----|------|----|
| | Quartus Prime Lite Edition (Free) 20.1.0.711 Installation Complete | | | |
| (intel? | Setup has finished installing Quartus Prime Lite Edition (Free) 20.1.0.711. Launch USB Blaster II driver installation Create shortcuts on Desktop Launch Quartus Prime Lite Edition Provide your feedback | | | |
| | | | | |
| | < Back Finit | sh | Cano | el |

Click "Ok", then click "Finish". The Quartus Prime is now installed and ready to be used.



| 🕞 Quartus Prime 20.1 Lite Edition | × |
|--|---|
| Thank you for installing the Quartus Prime software - the #1 in performance and productivity. T upgrade to a full featured edition, please https://www.intel.com/content/www/us/en/products/programmable.html. | o |
| Select one of the following licensing options to continue: | |
| Select one of the following options | |
| O Buy a Quartus Prime software license | |
| O Run the Quartus Prime software | |
| O Add an IP license file (for users who have purchased IP) | |
| OK Cancel | |

At this point the Quartus Prime Lite software is installed. Go to the Windows button and type in "quartus" at the search prompt.




The Windows Search should locate the installed version of Quartus. Click on the icon and the software should load properly. If this does not occur, contact Earth People Technology for support. There are three methods to contact EPT for support:

https://www.earthpeopletechnology.com->Forums support@earthpeopletechnology.com sales@earthpeopletechnology.com

> Page 109



7 Compiling and Synthesizing the FPGA Project



With the Quartus Prime Lite installed on the user PC, setting up and project and compiling and synthesizing is the next step. Once the user HDL code is written according to the syntax rules of the language (Verilog and VHDL) it can be compiled and synthesized using the Quartus Prime software. This manual will not focus on HDL coding or proper coding techniques, instead it will use the example code to compile, synthesize and program the FPGA.

7.1 Setting up the Project and Compiling

Once the HDL code (Verilog or VHDL) is written and verified using a simulator, a project can be created using Quartus Prime. Writing the HDL code and simulating it will be covered in later sections. Bring up Quartus Prime, then use Windows Explorer to browse to

C:\Users\nelso\Documents\ to create a new directory called:

"EPT_10CL016_AF_System_Demo".



Create another directory under the EPT_10CL016_AF_System_Demo called: EPT_10CL016_AF_T2_Top



| $\leftarrow \ \ \rightarrow \ \ \land \ \ \ \ \land \ \ \ \ \ \ $ | nelso > Documents > EPT_10CL0 | 016_AF_System_Demo | > | |
|--|-------------------------------|--------------------|-------------|------|
| ⊕ New ~ X □ □ □ △ ▷ □ ↓ Sort ~ ≡ View ~ | ••• | | | |
| > Cdssetup | Name | Date modified | Туре | Size |
| Contacts | EPT_10CL016_AF_T2_Top | 2/8/2025 2:55 PM | File folder | |
| > 📜 Cookies | | | | |
| Documents | | | | |
| > 📔 EPT_4CE6_AF_Platform_Demo | | | | |
| EPT_10CL016_AF_System_Demo | | | | |
| > EPT_10CL016_AF_T2_Top | | | | |
| > 🛃 My Music | | | | |
| > 📜 My Pictures | | | | |
| > 🗾 My Videos | | | | |
| > 📜 Visual Studio 2019 | | | | |

Open Quartus Prime by clicking on the icon.







Under Quartus, Select File->New Project Wizard. The Wizard will walk you through setting up files and directories for your project.





The "Introduction" window will open. Click "Next".



| S New Project Wizard | | | | Х |
|--|---|--|---|--------------------------------|
| Introduction | | | | |
| The New Project Wizard he and preliminary project se | elps you c ttings, inc | reate a I luding tl | new pro ne follov | ject wing: |
| Project name and di Name of the top-lev Project files and libr Target device family EDA tool settings rou can cnange the setting specify additional project- command (Assignments m pages of the Settings dialo the project Don't show me this interview | irectory rel design raries / and devid gs for an e wide settil nenu). You og box to a roduction | entity ce ngs with can use add func again | project a the Set the va tionality | ana ttings rious y to |
| Help | < <u>B</u> ack | <u>\</u> ext > | <u>F</u> inish | Cancel |

At the Top-Level Entity page, browse to the

 $C: Users \ EPT_10CL016_AF_System_Demo\ EPT_10CL016_AF_System_Demo\ mo$

directory to store your project. Type in a name for your project "EPT_10CL016_AF_T2_Top".



| New Project Wizard | × | | | | |
|--|-----|--|--|--|--|
| Directory, Name, Top-Level Entity | | | | | |
| What is the <u>w</u> orking directory for this project? | | | | | |
| CL016_AF_System_Demo/EPT_10CL016_AF_T2_Top | | | | | |
| What is the name of this <u>p</u> roject? | | | | | |
| EPT_10CL016_AF_T2_Top | | | | | |
| What is the name of the <u>t</u> op-level design entity for this project? This name is case sensitive and must exactly match the entity name in the design file. | | | | | |
| EPT_10CL016_AF_T2_Top . | | | | | |
| Use Existing Project Settings | | | | | |
| | | | | | |
| <u>H</u> elp < <u>B</u> ack <u>N</u> ext > <u>F</u> inish Can | cel | | | | |

Make sure you selected the "EPT_10CL016_AF_T2_Top" folder Select Next.

Choose the "Empty project"





Next, the "Add Files" window appears. Here we need to bring up a Windows Explorer window and browse to the

Size

C:\\$\\$Earth People Technology\CYCLOFLEX_FPGA_SYSTEM_PROJECT_1.0_DVD\Projects_HDL folder. ... Name > 📜 DLP Date modified Type Documentation 5/20/2023 10:28 PM File folder Earth People Technology Drivers 3/21/2023 10:26 PM File folder > BEEPROLOGIC_CPLD_DEV_SYS_PROJECT_1.0_DVD Projects_ActiveHost_64Bit 5/20/2023 10:28 PM File folder CYCLOFLEX_FPGA_SYSTEM_PROJECT_1.0_DVD Projects_HDL 5/20/2023 10:28 PM File folde Documentation Tutorials 3/21/2023 10:26 PM Drivers

 \leftarrow ↑ C 📮 > This PC > Windows (C:) > Jolly > Products > Earth People Technology > MEGAMAX_CPLD_SYSTEM_PROJECT_4.5_DVD >



In the Projects_HDL\EPT_10CL016_AF_System_Demo\src



folder of the EPT FPGA Development System DVD.

Q > ··· Earth People Technology > CYCLOFLEX_FPGA_SYSTEM_PROJECT_1.0_DVD >> Projects_HDL >> EPT_10CL016_CB_System_Demo >> $\leftarrow \rightarrow \land \Box$ Name CYCLOFLEX_FPGA_SYSTEM_PROJECT_1.0_DVD Date modified Туре Size Altera 1/22/2025 9:34 PM File folder Documentation EPT_10CL016_AF_T2_Top 1/22/2025 9:34 PM File folder Drivers 📒 ModelSim 1/22/2025 9:34 PM File folder > Projects_ActiveHost 🚞 sim 1/22/2025 9:34 PM File folder Projects_HDL src 💴 1/22/2025 9:34 PM File folder EPT_10CL016_CB_System_Demo 📜 test 1/22/2025 9:34 PM File folder 📒 Quartus_24.1_Prime 📒 Testbench 1/22/2025 9-34 PM File folder > 📒 Tutorials > DSO 100M DEV SYS PROJECT 2.8 DVD

Copy the files from the \scale{src} directory.

| New ~ 从 [] 〔〕 ④ [2] [2] 1↓ Sort ~ ■ | View ~ ··· | | | |
|---|---------------------------------------|---------------------|--------|--------|
| ✓ ➡ Earth People Technology | □ Name | Date modified | Туре | Size |
| BEEPROLOGIC_CPLD_DEV_SYS_PROJECT_1.0_DVD | ■ active_block.v | 3/2/2021 4:29 PM | V File | 10 KB |
| CYCLOFLEX_FPGA_SYSTEM_PROJECT_1.0_DVD | active_control_register.v | 3/2/2021 4:29 PM | V File | 4 KB |
| Documentation | active_spi_library.v | 1/21/2024 12:51 AM | V File | 7 KB |
| Drivers | active_transfer.v | 3/2/2021 4:29 PM | V File | 9 KB |
| Devices Astrophysics | active_transfer_spi.v | 1/22/2024 10:19 PM | V File | 27 KB |
| > Projects_ActiveHost | | 3/2/2021 4:29 PM | V File | 4 KB |
| ✓ Projects_HDL | Cycloprologic_define.v | 8/8/2021 8:12 PM | V File | 7 KB |
| EPT_10CL016_CB_System_Demo | i define.v | 11/11/2012 12:02 AM | V File | 3 KB |
| Cuartus_24.1_Prime | | 3/20/2021 4:34 PM | V File | 22 KB |
| > 🔁 Tutorials | EPT_10CL016_AF_T2_Top.v | 1/18/2025 10:19 PM | V File | 39 KB |
| > DSO_100M_DEV_SYS_PROJECT_2.8_DVD | ▲ eptWireOR.v | 7/5/2012 11:53 PM | V File | 2 KB |
| > DUEPROLOGIC_USB_FPGA_PROJECT_5.0_DVD | <pre> # ft_245_state_machine.v </pre> | 1/21/2024 11:34 PM | V File | 12 KB |
| > 📔 EPT I2C Project CD | 🛋 mem_array.v | 2/7/2012 2:05 PM | V File | 2 KB |
| > EPT Projects Folders | i≊∕ mux.v | 7/8/2013 3:37 PM | V File | 1 KB |
| | ▲ read_control_logic.v | 3/16/2012 10:15 AM | V File | 3 KB |
| ESP32_DJ_SNACK_PACK_PKUJECT_4.0_DVD | ▲ read_SPI_master.v | 1/3/2024 6:15 PM | V File | 7 KB |
| MAXPROLOGIC_FPGA_PROJECT_4.0_DVD | | 1/17/2025 7:10 DM | V/File | 14 1/1 |

- active_block.v
- active_control_register.v



- active_spi_library.v
- active_transfer.v
- active_transfer_spi.v
- active_trigger.v
- cycloprologic_define.v
- define.v
- endpoint_registers.v
- EPT_10CL016_AF_T2_Top.v
- eptWireOR.v
- ft_245_state_machine.v
- mem_array.v
- mux.v
- read_control_logic.v
- read_SPI_master.v
- rgb_led_control.v
- serial_clock.v
- seven_segment_led_display.v
- spi_iface_master.v
- sync_fifo.v
- write_control_logic.v
- write_SPI_master.v

Then paste them into a "src" folder on the C:\Users\nelso\Documents\EPT_10CL016_AF_System_Demo\src



| \leftarrow \rightarrow \uparrow \bigcirc \square \rightarrow This PC \rightarrow Windows (C:) \rightarrow Users \rightarrow | nelso > Documents > EPT_10CL0 | 16_AF_System_Demo | > src | |
|--|-------------------------------|----------------------|--------|---------|
| ⊕ New · | | | | |
| > 📜 .stmcufinder | Name | Date modified | Туре | Size |
| 3D Objects | 🗹 🚘 active_block.v | 3/2/2021 4:29 PM | V File | 10 KB |
| > 🦰 AppData | ☑ ≧ active_control_register.v | 3/2/2021 4:29 PM | V File | 4 KB |
| > 📜 Application Data | 🗹 🗟 active_spi_library.v | 1/21/2024 12:51 AM | V File | 7 KB |
| > cissetup | ☑ ≧ active_transfer.v | 3/2/2021 4:29 PM | V File | 9 KB |
| Casteda | active_transfer_spi.v | 1/22/2024 10:19 PM | V File | 27 KB |
| Contacts | ☑ ≧ active_trigger.v | 3/2/2021 4:29 PM | V File | 4 KB |
| > Ze Cookies | 🗹 🚘 cycloprologic_define.v | 8/8/2021 8:12 PM | V File | 7 KB |
| Documents | 🗹 🧟 define.v | 11/11/2012 12:02 AM | V File | 3 KB |
| > EPT_4CE6_AF_Platform_Demo | 🗹 🌌 endpoint_registers.v | 3/20/2021 4:34 PM | V File | 22 KB |
| EPT_10CL016_AF_System_Demo | EPT_10CL016_AF_T2_Top.v | 1/18/2025 10:19 PM | V File | 39 KB |
| src and a second | 🗹 🚘 eptWireOR.v | 7/5/2012 11:53 PM | V File | 2 KB |
| > 🥦 My Music | 🗹 📝 ft_245_state_machine.v | 1/21/2024 11:34 PM | V File | 12 KB |
| > 📜 My Pictures | 🗹 🚘 mem_array.v | 2/7/2012 2:05 PM | V File | 2 KB |
| > My Videos | 🗹 🚘 mux.v | 7/8/2013 3:37 PM | V File | 1 KB |
| > Viewel Studio 2010 | ☑ ≧ read_control_logic.v | 3/16/2012 10:15 AM | V File | 3 KB |
| | 🗹 🗟 read_SPI_master.v | 1/3/2024 6:15 PM | V File | 7 KB |
| > Downloads | | 4 /47 /2025 7-40 014 | ALCO. | 4.4.170 |

Then, go back to the Quartus "Add Files" window. Click on the "..." button across from the "File name:" textbox.



| | | | | | - | |
|-------------------------|------------------------|------------------------------------|---|---|---|---|
| | | | | | Add | |
| | | | | × | Add A | ٩ <u>I</u> I |
| Library Design Entry/Sy | ynthesis Tool | l HDL Version | | | Remo | ove |
| | | | | | Up | |
| | | | | | Dowr | |
| | | | | | 2011 | <u>.</u> |
| | | | | | Flobe | erue |
| | | | | | | |
| | | | | | | |
| | | | | | | |
| | | | | | | |
| | | | | | | |
| | Library Design Entry/S | Library Design Entry/Synthesis Too | Library Design Entry/Synthesis Tool HDL Version Remo Up Dowr Propr |

Navigate to the C:\Users\nelso\Documents\EPT_10CL016_AF_System_Demo\src folder



| Select File | | | | | |
|---|---|---------------------|--------|-------|---------------------|
| \leftarrow \rightarrow \checkmark \uparrow ${\frown}$ > This PC > Windows (C:) > Users > nelso > Docu | ments > EPT_10CL016_AF_System_Demo > sr | c | | ~ C | Search src |
| Organize • New folder | | | | | ≡ |
| Contacts | Name | Date modified | Туре | Size | |
| > 🚬 Cookies | | 3/2/2021 4:29 PM | V File | 10 KB | |
| Documents | □ 🖉 active_control_register.v | 3/2/2021 4:29 PM | V File | 4 KB | |
| EPT_4CE6_AF_Platform_Demo | 🗟 active_spi_library.v | 1/21/2024 12:51 AM | V File | 7 KB | |
| ✓ ► EPT 10CL016 AF System Demo | ☑ active_transfer.v | 3/2/2021 4:29 PM | V File | 9 KB | |
| | | 1/22/2024 10:19 PM | V File | 27 KB | |
| | | 3/2/2021 4:29 PM | V File | 4 KB | |
| > 🛃 My Music | 🛋 cycloprologic_define.v | 8/8/2021 8:12 PM | V File | 7 KB | i |
| > 🚬 My Pictures | i define.v | 11/11/2012 12:02 AM | V File | 3 KB | |
| > 🗦 My Videos | 📓 endpoint_registers.v | 3/20/2021 4:34 PM | V File | 22 KB | |
| > 📜 Visual Studio 2019 | EPT_10CL016_AF_T2_Top.v | 1/18/2025 10:19 PM | V File | 39 KB | |
| > 🖪 Downloads | | 7/5/2012 11:53 PM | V File | 2 KB | |
| > The Favorites | ft_245_state_machine.v | 1/21/2024 11:34 PM | V File | 12 KB | |
| | | | | | |
| File name: | | | | ~ | Design Files (*.tdf |
| | | | | | Open |

Then select all files in the "src" folder.

| Select File | | | | | | × |
|---|---|------------------------------|---------------------------|--------------------|-----------------------|--------------------------|
| \leftarrow \rightarrow \checkmark \uparrow This PC \Rightarrow Windows (C:) \Rightarrow Users \Rightarrow nelso \Rightarrow Doc | uments > EPT_10CL016_AF_System_Demo > src | | | ~ C | Search src | م |
| Organize - New folder | | | | | ≡ | · 🗆 🕜 |
| Contacts | □ Name | Date modified | Туре | Size | | |
| > 📜 Cookies | ☑ 🛃 active_block.v | 3/2/2021 4:29 PM | V File | 10 KB | | |
| ✓ ■ Documents | active_control_register.v | 3/2/2021 4:29 PM | V File | 4 KB | | |
| > EPT_4CE6_AF_Platform_Demo | ☑ 	 active_spi_library.v | 1/21/2024 12:51 AM | V File | 7 KB | | |
| EPT 10CL016 AF System Demo | ☑ ▲ active_transfer.v | 3/2/2021 4:29 PM | V File | 9 KB | | |
| | ☑ ▲ active_transfer_spi.v | 1/22/2024 10:19 PM | V File | 27 KB | | |
| | ☑ ▲ active_trigger.v | 3/2/2021 4:29 PM | V File | 4 KB | | No preview available. |
| > My Music | 🖻 🗟 cycloprologic_define.v | 8/8/2021 8:12 PM | V File | 7 KB | | |
| > 2 My Pictures | 🛃 🌌 define.v | 11/11/2012 12:02 AM | V File | 3 KB | | |
| > 🛃 My Videos | ✓ | 3/20/2021 4:34 PM | V File | 22 KB | | |
| > 📜 Visual Studio 2019 | EPT_10CL016_AF_T2_Top.v | 1/18/2025 10:19 PM | V File | 39 KB | | |
| > 🚺 Downloads | ☑ ≧ eptWireOR.v | 7/5/2012 11:53 PM | V File | 2 KB | | |
| > 🦰 Favorites | ☑ ▲ ft_245_state_machine.v | 1/21/2024 11:34 PM | V File | 12 KB | | |
| File name: "write_SPI_master.v" "active_block.v" "active_cor | trol_register.v" "active_spi_library.v" "active_transfer. | v" "active_transfer_spi.v" " | active_trigger.v" "cyclop | rologic_define.v × | Design Files (*.tdf * | .vhd *.vhdl *.v ~ |
| | | | | | | |



Click "Open"

| Note: you can always add design files to | o the project later. | | |
|--|----------------------|--------------------------------|------------|
| ile name: | | | Add |
| • | | × | Add All |
| File Name | Туре | Library Design Entry/Synthesis | Remove |
| src/write_SPI_master.v | Verilog HDL File | | Temote |
| src/write_control_logic.v | Verilog HDL File | | <u>U</u> p |
| src/sync_fifo.v | Verilog HDL File | | Down |
| src/spi_liace_master.v | Verilog HDL File | | Domi |
| src/seven_segment_ted_display.v | Verilog HDL File | | Propertie: |
| src/rgb led control.v | Verilog HDL File | | |
| src/read SPI master.v | Verilog HDL File | | |
| src/read_control_logic.v | Verilog HDL File | | |
| src/mux.v | Verilog HDL File | | |
| src/mem_array.v | Verilog HDL File | | |
| <pre>src/ft_245_state_machine.v</pre> | Verilog HDL File | | |
| src/eptWireOR.v | Verilog HDL File | | |
| src/EP1_10CL016_AF_12_10p.v | Verilog HDL File | - | |

Now, all source files for the project are in the Quartus Prime project.

Select Next, at the Device Family group, select Cyclone 10 for Family. In the Available Devices group, browse down to 10CL016YE144C8G for Name.



| Device Board | | | | | | | |
|---|---|---|---|---|---|---|-----|
| Select the family and device y | ou want to target for com | pilation. | . command on | the Teels m | | | |
| To determine the version of th | ne Quartus Prime softwar | re in whice | h your target c | device is sup | ported, refer to t | the <u>Device Support List</u> web | opa |
| Device family | | | Show in | 'Available d | levices' list | | |
| Family: Cyclone 10 LP | | | • | | | | |
| Dovice: All | | Pac <u>k</u> age: | | | Any | | * |
| Device: All | | * | | | Any | | ۳ |
| Target device | arget device | | | sp <u>e</u> ed grade | : Any | | ٣ |
| Auto device selected by the Fitter | | | Name | filter: | | | |
| Specific device selected Other: n/a | in 'Available devices' list | | √ S <u>h</u> | iow advance | d devices | | |
| Specific device selected Other: n/a Available devices: Name | in 'Available devices' list Core Voltage | LEs | ✓ Sh | ow advance | d devices | Embedded multiplier | 9-b |
| Specific device selected Other: n/a Available devices: Name 10CL010YU256C8G | in 'Available devices' list Core Voltage 1.2V | LEs 10320 | ✓ Sh Total I/Os 177 | GPIOs | Memory Bits 423936 | Embedded multiplier 9 | 9-b |
| Specific device selected Other: n/a Available devices: Name 10CL010YU256C8G 10CL010YU256I7G | in 'Available devices' list Core Voltage 1.2V 1.2V | LEs 10320 10320 | ✓ Sh Total I/Os 177 177 | GPIOs 177 177 | Memory Bits 423936 423936 | Embedded multiplier 9 46 46 | 9-b |
| Specific device selected Other: n/a Available devices: Name 10CL010YU256C8G 10CL010YU256I7G 10CL010ZE144I8G | in 'Available devices' list Core Voltage 1.2V 1.2V 1.0V | LEs 10320 10320 10320 | ▼ Sh Total I/Os 177 177 89 | GPIOs 177 177 89 | Memory Bits 423936 423936 423936 | Embedded multiplier 46 46 46 | 9-b |
| Specific device selected Other: n/a Available devices: Name 10CL010YU256C8G 10CL010ZE144I8G 10CL010ZE144I8G 10CL010ZM164I8G | in 'Available devices' list Core Voltage 1.2V 1.2V 1.0V 1.0V | LEs 10320 10320 10320 10320 | ▼ Sh Total I/Os 177 177 89 102 | GPIOs 177 177 89 102 | Memory Bits 423936 423936 423936 423936 423936 | Embedded multiplier 46 46 46 46 | 9-b |
| Specific device selected Other: n/a Available devices: Name 10CL010YU256C8G 10CL010ZE144I8G 10CL010ZE144I8G 10CL010ZM164I8G 10CL010ZU256I8G | in 'Available devices' list Core Voltage 1.2V 1.2V 1.0V 1.0V 1.0V 1.0V | LEs 10320 10320 10320 10320 10320 | ▼ Sh Total I/Os 177 177 89 102 177 | GPIOs 177 177 89 102 177 | Memory Bits 423936 423936 423936 423936 423936 423936 423936 423936 | Embedded multiplier 46 46 46 46 46 46 | 9-b |
| Specific device selected Other: n/a Available devices: Name 10CL010YU256C8G 10CL010ZE144I8G 10CL010ZM164I8G 10CL010ZU256I8G 10CL016YE144A7G | in 'Available devices' list Core Voltage 1.2V 1.2V 1.0V 1.0V 1.0V 1.0V 1.2V | LEs 10320 10320 10320 10320 10320 15408 | ▼ Sh Total I/Os 177 177 89 102 177 79 | GPIOs 177 177 89 102 177 9 | Memory Bits 423936 423936 423936 423936 423936 516096 | Embedded multiplier 9 46 46 46 46 46 46 46 112 | 9-b |
| Specific device selected Other: n/a Available devices: Name 10CL010YU256C8G 10CL010ZE144I8G 10CL010ZE144I8G 10CL010ZU256I8G 10CL016YE144A7G 10CL016YE1444C6G | in 'Available devices' list Core Voltage 1.2V 1.2V 1.0V 1.0V 1.0V 1.2V 1.2V 1.2V 1.2V | LEs 10320 10320 10320 10320 10320 15408 15408 | ▼ Sh Total I/Os 177 177 89 102 177 79 79 79 | GPIOs 177 177 89 102 177 9 79 79 | Memory Bits 423936 423936 423936 423936 423936 516096 516096 | Embedded multiplier 9 46 46 46 46 46 46 112 112 | 9-b |
| Specific device selected Qther: n/a Ayailable devices: Name 10CL010YU256C8G 10CL010ZE144I8G 10CL010ZE144I8G 10CL010ZU256I8G 10CL016YE144A7G 10CL016YE1444C6G 10CL016YE144C6G 10CL016YE144C8G | in 'Available devices' list Core Voltage 1.2V 1.2V 1.0V 1.0V 1.0V 1.2V 1.2V 1.2V 1.2V 1.2V | LEs 10320 10320 10320 10320 10320 15408 15408 15408 | ▼ Sh Total I/Os 177 177 89 102 177 79 79 79 | GPIOs 477 477 477 89 402 477 79 79 79 79 | Memory Bits 423936 423936 423936 423936 423936 516096 516096 516096 | Embedded multiplier 9 46 46 46 46 46 46 112 112 112 | 9-b |
| Specific device selected Qther: n/a Available devices: Name 10CL010YU256C8G 10CL010ZE14418G 10CL010ZE14418G 10CL010ZU25618G 10CL016YE144A7G 10CL016YE1444C6G 10CL016YE14447G 10CL016YE14417G | in 'Available devices' list Core Voltage 1.2V 1.2V 1.2V 1.0V 1.0V 1.0V 1.2V 1.2V 1.2V 1.2V 1.2V 1.2V 1.2V | LEs 10320 10320 10320 10320 10320 15408 15408 15408 | ▼ Sh Total I/Os 177 177 89 102 177 79 79 79 79 79 79 | CPIOS GPIOS 177 177 89 102 177 79 79 79 79 79 | Memory Bits 423936 423936 423936 423936 423936 516096 516096 516096 516096 516096 | Embedded multiplier 9 46 46 46 46 46 46 112 112 112 112 112 | 9-b |
| Specific devices selected Qther: n/a Ayailable devices: Name 10CL010YU256C8G 10CL010ZE14418G 10CL010ZE14418G 10CL010ZU25618G 10CL016YE144A7G 10CL016YE14447G 10CL016YE14447G 10CL016YE14417G 10CL016YF484C6G | in 'Available devices' list Core Voltage 1.2V 1.2V 1.2V 1.0V 1.0V 1.0V 1.2V 1.2V 1.2V 1.2V 1.2V 1.2V 1.2V 1.2V | LEs 10320 10320 10320 10320 10320 15408 15408 15408 15408 | ▼ Sh Total I/Os 177 177 89 102 177 79 79 79 79 341 | GPIOs 177 177 177 102 177 79 79 79 341 | Memory Bits 423936 423936 423936 423936 423936 516096 516096 516096 516096 516096 516096 516096 | Embedded multiplier 9 46 46 46 46 46 112 112 112 112 112 112 | 9-b |
| Specific devices selected Qther: n/a Ayailable devices: Name 10CL010YU256C8G 10CL010ZE14418G 10CL010ZE14418G 10CL010ZU25618G 10CL016YE144A7G 10CL016YE14447G 10CL016YE14447G 10CL016YE14417G 10CL016YF484C6G 10CL016YF484C8G | in 'Available devices' list Core Voltage 1.2V 1.2V 1.2V 1.0V 1.0V 1.0V 1.2V 1.2V 1.2V 1.2V 1.2V 1.2V 1.2V 1.2V 1.2V | LEs 10320 10320 10320 10320 10320 15408 15408 15408 15408 15408 | ▼ Sh Total I/Os 177 177 177 102 177 79 79 341 341 | GPIOs 177 177 177 102 177 79 79 341 341 | Memory Bits 423936 423936 423936 423936 423936 516096 516096 516096 516096 516096 516096 516096 516096 516096 | Embedded multiplier 9 46 46 46 46 46 112 112 112 112 112 112 112 112 | 9-b |

Select Next, leave defaults for the EDA Tool Settings.



| ool Type esign Entry/Syr | Tool Name | | | |
|-----------------------------|---------------------|---------------|---|--|
| esign Entry/Sy | | Format(s) | | Run Tool Automatically |
| 0 | n <none></none> | <none></none> | * | Run this tool automatically to synthesize the current design |
| mulation | Questa Intel FPGA 🔹 | Verilog HDL | ٣ | Run gate-level simulation automatically after compilation |
| oard-Level | Timing | <none></none> | ۳ | |
| | Symbol | <none></none> | ۳ | |
| | Signal Integrity | <none></none> | ۳ | |
| | Boundary Scan | <none></none> | • | |
| | | | | |

Select Next, then select Finish. You are done with the project level selections.



| Summary | |
|--|---|
| When you click Finish, the project will be created w | ith the following settings: |
| Project directory: | C:\Users\nelso\Documents\EPT_10CL016_AF_System_Demo |
| Project name: | EPT_10CL016_AF_T2_Top |
| Top-level design entity: | EPT_10CL016_AF_T2_Top |
| Number of files added: | 23 |
| Number of user libraries added: | 0 |
| Device assignments: | |
| Design template: | n/a |
| Family name: | Cyclone 10 LP |
| Device: | 10CL016YE144C8G |
| Board: | n/a |
| EDA tools: | |
| Design entry/synthesis: | <none> (<none>)</none></none> |
| Simulation: | Questa Intel FPGA (Verilog HDL) |
| Timing analysis: | 0 |
| Operating conditions: | |
| VCCINT voltage: | 1.2V |
| Junction temperature range: | 0-85 � C |
| | |
| | |
| | |
| | |
| | |
| <u>H</u> elp | < <u>Back</u> <u>Next</u> > <u>Finish</u> Cancel |

Now, your project is ready to go.



| | U X |
|---|-----------------|
| File Edit View Project Assignments Processing Tools Window Help | th Intel ERGA |
| | IT IIItet FF GA |
| | Ter |
| Project Navigator A Hierarchy V 2000 | × × |
| Entitylinstance | |
| <pre>vpcione io UP: iouCollete LakeBig v EDT iouCollete A to Tan^h v Project Directory</pre> | |
| No Selection Available | |
| ▼ Library | |
| Basic Functions | |
| b DSP | |
| Interface protocols Memory Interfaces and Co | ntrollers |
| Promy interaction of the second se | s |
| Quartus Prime Vulversity Program | |
| Search for Partner IP Search for Partner IP | |
| Tasks Compilation Version 23.1 Lite Edition | |
| Task | |
| Compile Design | |
| Analysis & Synthesis | |
| Filter (value & koule) | |
| Assembler (derivate progr w for solver) w for solver) | |
| Construction Construction Construction | |
| + Add_ | |
| All O A A Y < <filter>> 68 Find, #Find Next</filter> | |
| | |
| lybe in wessage | |
| | |
| | Þ |
| System Processing | |
| 2 | 6 00:00:00 |

Next, we will select the pins and synthesize the project.

7.1.1 Selecting Pins and Synthesizing

With the project created, we need to assign pins to the project. The signals defined in the top level file (in this case: EPT_10CL016_AF_T2_Top.v) will connect directly to pins on the FPGA. The Pin Planner Tool from Quartus Prime will add the pins and check to verify that our pin selections do not violate any restrictions of the device. In the case of this example we will import pin assignments that created at an earlier time. Under Assignments, Select Import Assignments.



| 🕥 Quartus Prime Lite Editi | on - C:/Users/nelso/Documents/EPT_100 | CL016_AF_System_D | emo/EPT_10CL016_AF_T2_Top/EPT_10CL016_AF_T2_Top - EPT_10 |
|-------------------------------|--|-------------------|--|
| <u>Eile Edit View Project</u> | Assignments Processing Tools Win | dow <u>H</u> elp | |
| | <u>D</u>evice <u>S</u>ettings | Ctrl+Shift+E | ♥ ♣ ♥ 🚺 🛛 ♥ |
| Project Navigator 🔺 Hierar | < <u>A</u> ssignment Editor | Ctrl+Shift+A | |
| Entity:Instan | 🗳 Pi <u>n</u> Planner | Ctrl+Shift+N | |
| Cyclone 10 LP: 10CL016Y | <u>R</u> emove Assignments | | |
| EPT_10CL016_AF_T2 | <u>Back-Annotate Assignments</u> | | |
| | Imp <u>o</u> rt Assignments | | |
| | E <u>x</u> port Assignments | | |
| | Assignment <u>G</u> roups | | |
| | Logic Lock Regions Window | Alt+L | |
| | Design Partitions <u>W</u> indow | Alt+D | |
| Tasks Compilation | ▼ ■ ¥ 0 8 | | Quartus Prime Version 23.1 Lite Edition |
| | Task | | |
| 🔻 🕨 Compile Design | | | |
| 🕨 🕨 Analysis & S | ynthesis | | |
| 🕨 🕨 Fitter (Place | & Route) | | |
| 🕨 🕨 Assembler (| Generate progr | | |
| 🕨 🕨 Timing Anal | ysis | | |
| | M/sites | | |

At the Import Assignment dialog box, Browse to the $Projects_HDL EPT_System_Demo \\ EPT_10CL016_AF_T2_TOP folder of the EPT FPGA Development System DVD. Select the "EPT_10CL016_AF_T2_Top.qsf" file.$



| Select File | | | | | | × |
|---|--|-----------------------|---------------|------|-------------------------|------------------------------|
| \leftarrow \rightarrow \checkmark \uparrow \sim \uparrow \sim \uparrow \sim CYCLOFLEX_FPGA_SYSTEM_PROJECT_1.0_DVD \rightarrow P | rojects_HDL > EPT_10CL016_CB_System_Demo > | EPT_10CL016_AF_T2_Top | • | ~ C | Search EPT_10CL016 | 5_AF_T2_T P |
| Organize - New folder | | | | | ≡ | · 🔲 🕜 |
| Drivers | Name | Date modified | Туре | Size | | |
| > Projects_ActiveHost | 📜 db | 1/22/2025 9:34 PM | File folder | | | |
| Projects_HDL | incremental_db | 1/22/2025 9:34 PM | File folder | | | |
| EPT_10CL016_CB_System_Demo | output_files | 1/22/2025 9:34 PM | File folder | | | |
| Altera | EPT_10CL016_AF_T2_Top.qsf | 1/18/2025 10:19 PM | QSF File | 9 KB | | |
| > EPT_10CL016_AF_T2_Top | EPT_10CL016_AF_T2_Top.sdc | 10/21/2023 10:06 PM | SDC File | 4 KB | | |
| > Contraction > | EPT_10CL016_AF_T2_Top_description.txt | 4/2/2021 6:48 PM | Text Document | 0 KB | | Select a file to preview. |
| 🚬 sim | | | | | | |
| src 🔁 | | | | | | |
| test 🔁 | | | | | | |
| Testbench | | | | | | |
| Cuartus_24.1_Prime | | | | | | |
| | | | | | | |
| File name: | | | | ~ | Import Files (*.qsf *.e | esf *.acf *.csv ~ |
| | | | | | Open | Cancel |

Click "Open"





Click Ok. Under Assignments, Select Pin Planner. Verify the pins have been imported correctly.



| 🕥 Quartus Prime Lite Edition - C:/Users/ | nelso/Documents/EPT_10CL01 | 6_AF_System_De | emo/EPT_10CL01 | 16_AF_T2_Top/EPT_10CL016_AF_T2_Top - El | PT_10CL016_AF_T2_Top |
|--|--|----------------|----------------|---|----------------------|
| <u>File Edit View Project</u> Assignments | P <u>r</u> ocessing <u>T</u> ools <u>W</u> indow | / <u>H</u> elp | | | |
| ▶ <u>D</u> evice ▶ <u>D</u> evice ▶ <u>D</u> evice ▶ <u>D</u> evice | • | Ctrl+Shift+E | S 7 🖗 | 9 | |
| Project Navigator 🔺 Hierar 🎸 Assignme | ent Editor | Ctrl+Shift+A | | | |
| Entity:Instan 🍼 Pi <u>n</u> Planr | ner | Ctrl+Shift+N | | | |
| Cyclone 10 LP: 10CL016Y <u>R</u> emove | Assignments | | | | |
| EPT_10CL016_AF_T2 Back-Ann | notate Assignments | | | | |
| Imp <u>o</u> rt As | ssignments | | | | |
| E <u>x</u> port As | ssignments | | | | |
| Assignme | ent <u>G</u> roups | | | | |
| ▲ Logic Loc | k Regions Window | Alt+L | | | |
| Design P | artitions <u>W</u> indow | Alt+D | | | |
| | - | | | Quartus Prime | |
| Tasks Compilation 🔻 🗉 | | | | | |
| Task | | | | | |
| Compile Design | | | | | |
| Analysis & Synthesis | | | | | |
| Fitter (Place & Route) | | | | | |
| Assembler (Generate prog | gr | | | | |
| Timing Analysis | | | | | |
| EDA Netlist Writer | v | | | | |
| 4 | | | | | |

The pin locations should not need to be changed for EPT USB FPGA Development System. However, if you need to change any pin location, just click on the "location" column for the particular node you wish to change. Then, select the new pin location from the drop down box.



| eport | | ¥@ 8 | | 1474(4) | 4 4 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 2 3 2 | 201111111111111111111111111111111111111 | | | Pin Legend |
|----------------------------------|----------------|----------|----------|-------------------------|--|---|------------------|-----------|---|
| Report not available | | | | | Top Viev Bond, with Ex | v posed P | 9 | | Symbol Pin Ty User I User z Fitter |
| Groups Report | | | | 18M 19 200 212 | | 1091 1009 1009 1008 1008 | | | Unbor Reser |
| asks | | ₹@≈ | | 23 24 25 25 | Cyclone 10 | LP | | | C Other |
| 🔻 🆻 Early Pin Planning | | | | 20. 10 | 10CI 016YE14 | 14C8G 🖉 | | | E DEV_0 |
| Early Pin Plan | ning | | | 31 A 32 - 33 - | ICCLOICIEI | 178 178 178 | | | R DEV |
| Run I/O Assia | nment Analysis | | | 34 35A 36A | | 479 474 73 | | | |
| Export Pin Ass | , ignments | Ŧ | | 373039 | 104 14 24 34 44 54 64 74 64 15 05 15 25 35 46 55 65 75 05 96 | 0 1.5.5.0-0546.7600000172 | | | 4 |
| 🚪 Named: * 🔻 🌯 Edit: 🗵 | ~ | | | | | | | | Filter: Pins: all |
| * Node Name | Direction | Location | I/O Bank | VREF Group | I/O Standard | Reserved | Current Strength | Slew Rate | Differential Pair Stri |
| USER_LEDS[0] | Unknown | PIN_10 | 1 | B1_N1 | 2.5 V (default) | | 8mA (default) | | |
| USER_LEDS[3] | Unknown | PIN_42 | 3 | B3_N1 | 2.5 V (default) | | 8mA (default) | | |
| USER_LEDS[4] | Unknown | PIN_114 | 7 | B7_N0 | 2.5 V (default) | | 8mA (default) | | |
| USER_LEDS[5] | Unknown | PIN_112 | 7 | B7_N0 | 2.5 V (default) | | 8mA (default) | | |
| USER_LEDS[6] | Unknown | PIN_113 | 7 | B7_N0 | 2.5 V (default) | | 8mA (default) | | |
| USER_LEDS[7] | Unknown | PIN_106 | 6 | B6_N0 | 2.5 V (default) | | 8mA (default) | | |
| RST_N | Unknown | PIN_87 | 5 | B5_N0 | 2.5 V (default) | | 8mA (default) | | |
| CLK_50MHZ | Unknown | PIN_22 | 1 | B1_N1 | 2.5 V (default) | | 8mA (default) | | |
| USER_LEDS[1] | Unknown | PIN_32 | 2 | B2_N1 | 2.5 V (default) | | 8mA (default) | | |
| USER_LEDS[2] | Unknown | PIN_33 | 2 | B2_N1 | 2.5 V (default) | | 8mA (default) | | |
| PB_SWITCH_2 | Unknown | PIN_91 | 6 | B6_N1 | 2.5 V (default) | | 8mA (default) | | |
| PB_SWITCH_1 | Unknown | PIN_126 | 7 | B7_N1 | 2.5 V (default) | | 8mA (default) | | |
| SPI_SCLK | Unknown | PIN_125 | 7 | B7_N1 | 2.5 V (default) | | 8mA (default) | | |
| SPI_SS | Unknown | PIN_121 | 7 | B7_N1 | 2.5 V (default) | | 8mA (default) | | |
| SPI_MISO | Unknown | PIN_115 | 7 | B7_N0 | 2.5 V (default) | | 8mA (default) | | |
| SPI_MIOSIO_1 | Unknown | PIN_120 | 7 | B7_N1 | 2.5 V (default) | | 8mA (default) | | |
| RGB_LED_GREEN | Unknown | PIN_49 | 3 | B3_N0 | 2.5 V (default) | | 8mA (default) | | |
| RGB_LED_BLUE | Unknown | PIN_44 | 3 | B3_N1 | 2.5 V (default) | | 8mA (default) | | |
| • RGB LED RED | Unknown | PIN 43 | 3 | B3 N1 | 2.5 V (default) | | 8mA (default) | | |
| LED_DISPLAY_1[7] | Unknown | PIN_142 | 8 | B8_N1 | 2.5 V (default) | | 8mA (default) | | |
| LED_DISPLAY_1[6] | Unknown | PIN_141 | 8 | B8_N1 | 2.5 V (default) | | 8mA (default) | | |
| LED_DISPLAY_1[5] | Unknown | PIN_135 | 8 | B8_NO | 2.5 V (default) | | 8mA (default) | | |
| LED DISPLAY 1[4] | Unknown | PIN_137 | 8 | B8 NO | 2.5 V (default) | | 8mA (default) | | |
| LED_DISPLAY_1[3] | Unknown | PIN_136 | 8 | B8_NO | 2.5 V (default) | | 8mA (default) | | |
| LED_DISPLAY_1[2] | Unknown | PIN_143 | 8 | B8_N1 | 2.5 V (default) | | 8mA (default) | | |
| LED_DISPLAY_1[1] | Unknown | PIN_144 | 8 | B8_N1 | 2.5 V (default) | | 8mA (default) | | |
| LED_DISPLAY_1[0] | Unknown | PIN_133 | 8 | B8_N0 | 2.5 V (default) | | 8mA (default) | | |
| LED_DISPLAY_3[7] | Unknown | PIN_105 | 6 | B6_N0 | 2.5 V (default) | | 8mA (default) | | |
| LED_DISPLAY_3[6] | Unknown | PIN_100 | 6 | B6_N1 | 2.5 V (default) | | 8mA (default) | | |
| LED_DISPLAY_3[5] | Unknown | PIN_99 | 6 | B6_N1 | 2.5 V (default) | | 8mA (default) | | |
| LED_DISPLAY_3[4] | Unknown | PIN_101 | 6 | B6_N1 | 2.5 V (default) | | 8mA (default) | | |
| LED_DISPLAY_3[3] | Unknown | PIN_103 | 6 | B6_N1 | 2.5 V (default) | | 8mA (default) | | |
| | Links area | DIN 444 | 7 | D7 NO | 253444-6-14 | | Ome A (defeuile) | | |

Exit the Pin Planner. Next, we need to add the Synopsys Design Constraint file. This file contains timing constraints which forces the built in tool called TimeQuest Timing Analyzer to analyze the path of the synthesized HDL code with setup and hold times of the internal registers. It takes note of any path that may be too long to appropriately meet the timing qualifications. For more information on TimeQuest Timing Analyzer, see

Quest Timing Analyzer Quick Start Guide



Browse to the \Projects_HDL\EPT_Platform_Demo \ EPT-10CL016-AF-T2_TOP folder of the EPT FPGA Development System DVD. Select the "EPT_10CL016_AF_T2_Top.sdc" file.

| \leftarrow \rightarrow \uparrow \bigcirc \square \rightarrow \cdots CYCLOFLEX_FPGA_SYSTEM_PROJECT_1.0_E | DVD > Projects_HDL > EPT_10CL0 | 16_CB_System_Demo | > EPT_10CL016_A | F_T2_Top > |
|---|---------------------------------------|---------------------|--------------------|------------|
| ⊕ New ~ | | | | |
| > DLP | □ Name | Date modified | Туре | Size |
| ✓ ► Earth People Technology | 📜 db | 1/22/2025 9:34 PM | File folder | |
| >BEEPROLOGIC_CPLD_DEV_SYS_PROJECT_1.0_DVD | 📁 incremental_db | 1/22/2025 9:34 PM | File folder | |
| CYCLOFLEX_FPGA_SYSTEM_PROJECT_1.0_DVD | output_files | 1/22/2025 9:34 PM | File folder | |
| Documentation | EPT_10CL016_AF_T2_Top.cdf | 10/21/2023 1:48 AM | CDF File | 1 KB |
| | EPT_10CL016_AF_T2_Top.map | 8/3/2021 12:35 AM | Linker Address Map | 1 KB |
| Drivers | EPT_10CL016_AF_T2_Top.qpf | 4/2/2021 6:48 PM | QPF File | 2 KB |
| > Projects_ActiveHost | EPT_10CL016_AF_T2_Top.qsf | 1/18/2025 10:19 PM | QSF File | 9 KB |
| V Projects_HDL | EPT_10CL016_AF_T2_Top.sdc | 10/21/2023 10:06 PM | SDC File | 4 KB |
| EPT_10CL016_CB_System_Demo | EPT_10CL016_AF_T2_Top_assignment | 9/25/2024 10:34 PM | QDF File | 55 KB |
| Quartus_24.1_Prime | EPT_10CL016_AF_T2_Top_description.txt | 4/2/2021 6:48 PM | Text Document | 0 KB |
| > 📜 Tutorials | | | | |
| | | | | |

Copy the file and browse to

 $\label{eq:c:list} C:\label{eq:c:list} C:\lab$

directory. Paste the file.



| $\leftarrow \ \ \rightarrow \ \ \land \ \ \bigcirc \ \ $ | nelso > Documents > EPT_10CL | 016_AF_System_Demo | > EPT_10CL016 | _AF_T2_Top > | Search |
|---|-------------------------------|---------------------|---------------|--------------|--------|
| ⊕ New · | <i>y</i> ~ •••• | | | | |
| > 🦰 AppData | □ Name | Date modified | Туре | Size | |
| > 🚬 Application Data | 📒 db | 2/8/2025 3:11 PM | File folder | | |
| > 🔁 cdssetup | EPT_10CL016_AF_T2_Top.qpf | 2/8/2025 3:06 PM | QPF File | 2 KB | |
| Contacts | EPT_10CL016_AF_T2_Top.qsf | 2/8/2025 3:06 PM | QSF File | 5 KB | |
| > 📜 Cookies | EPT_10CL016_AF_T2_Top.qsf.bak | 2/8/2025 3:10 PM | BAK File | 5 KB | |
| Documents | EPT_10CL016_AF_T2_Top.sdc | 10/21/2023 10:06 PM | SDC File | 4 KB | |
| > EPT_4CE6_AF_Platform_Demo | | | | | |
| EPT_10CL016_AF_System_Demo | | | | | |
| >EPT_10CL016_AF_T2_Top | | | | | |
| src Src | | | | | |
| > 🗦 My Music | | | | | |
| > 🚬 My Pictures | | | | | |
| N Net Videor | | | | | |

Select the Start Compilation button.





If you forget to include a file or some other error you should expect to see a screen similar to this:



| 🕞 Quartus Prime Lite Edition - C:/Jolly/Code_FPGA | /EPT_4CE6_AF_Data_Collector_2/EPT_4C | CE6_AF_D1_Top - EPT_4CE6_AF | _D1_Top | - 0 | × |
|--|--|-----------------------------|---|---|----------|
| <u>Eile Edit View Project Assignments Proc</u> | essing <u>T</u> ools <u>W</u> indow <u>H</u> elp | | | Search altera.com | 9 |
| D to U + D to C EPT_4CE6_ | AF_D1_Top 🔹 🖌 🇳 🗳 | 🗞 💷 🕨 🗶 🐥 🛛 | 🗢 🛦 🔌 🚂 🗢 | | |
| Project Navigator 🔥 Hierarchy 🔹 🔍 🛄 🗗 🗙 | Compilation Report - EPT_4 | ICE6_AF_D1_Top | | IP Catalog | 8 × |
| Entity:Instance | Table of Contents 🛛 📮 🗗 | Flow Summary | | × | Ę |
| Cyclone IV E: EP4CE6E22C8 | 📰 Flow Summary | < <filter>></filter> | | 🗸 🙀 Installed IP | ^ |
| EPT 4CE6 AF D1 Top 4 | == Flow Settings | Flow Status | Flow Failed - Sun Aug 09 20:42:17 2020 | Y Project Directory | |
| | == Flow Non-Default Global Set | Quartus Prime Version | 20.1.0 Build 711 06/05/2020 SJ Lite Edition | No Selection Available | |
| | Flow Elapsed Time | Revision Name | EPT_4CE6_AF_D1_Top | ✓ Library | |
| | = Flow OS Summary | Top-level Entity Name | EPT_4CE6_AF_D1_Top | > Basic Functions | |
| | Flow Log | Family | Cyclone IV E | > DSP | |
| Tasks Compilation • = 4 B* * | 🗦 📕 Analysis & Synthesis | Device | EP4CE6E22C8 | > Interface Protocols | |
| Task | Flow Messages | Timing Models | Final | Processors and Peripherals | |
| 🗙 👻 🕨 Compile Design | Flow Suppressed Messages | Total logic elements | N/A until Partition Merge | > University Program | |
| X > Analysis & Synthesis | | Total registers | N/A until Partition Merge | Search for Partner IP | ~ |
| < | < > | Total pins | N/A until Partition Merge | + Add | |
| × | | | N/A until Partition Merge | , | |
| All S ▲ ▲ ▼ < <filter>></filter> | | 💏 Eind 💏 Find N | e <u>x</u> t | | |
| Type ID Message | | | | | ^ |
| 18236 Number of processor | s has not been specified w | which may cause over | loading on shared machines. Set the globa | <pre>1 assignment NUM_PARALLEL_PROCES</pre> | 50 |
| 20030 Parallel compilatio | n is enabled and will use | 2 of the 2 processo | rs detected | | |
| 12021 Found 1 design unit | s, including 1 entities, i s. including 1 entities, i | in source file src/e | t_245_state_machine.v | | |
| 🗙 10170 Verilog HDL syntax | error at EPT_4CE6_AF_D1_To | p.v(115) near text: | "wire"; expecting ";". Check for and fix | any syntax errors that appear in | nr |
| 10112 Ignored design unit | "EPT_4CE6_AF_D1_Top" at E | PT_4CE6_AF_D1_Top.v | (35) due to previous errors | | |
| 12021 Found 0 design unit | s, including 0 entities, i | in source file src/e | pt_4ce6_af_d1_top.v | | |
| 12021 Found 1 design unit | s, including I entities, i s. including 0 entities. i | in source file src/e | efine.v | | |
| 8 12021 Found 1 design unit | s. includina 1 entities. i | in source file src/a | ctive triaaer.vam | | ~ |
| 8 | | | | 3 | <u>}</u> |
| ^δ / _Σ System (3) Processing (20) | | | | | |
| | | | | 2% 00:00:1 | 15 .: |

Click Ok, the select the "Error" tab to see the error.



| S Quartus Prime Lite Edition - C:/Jolly/Code_FPGA | /EPT_4CE6_AF_Data_Collector_2/EPT_4C | E6_AF_D1_Top - EPT_4CE6_AF | _D1_Top | | | × |
|---|---|----------------------------|---|-------------|--------------------------------|--------------|
| <u>File Edit View Project Assignments Proc</u> | essing <u>T</u> ools <u>W</u> indow <u>H</u> elp | | | | Search altera.com | 9 |
| D 🔽 🖶 🗲 🗅 💼 つ C EPT_4CE6_/ | AF_D1_Top 🛛 👻 🏑 🗳 🗳 | 🚸 💷 🕨 🖌 🤘 🤅 | 9 & & 🧱 🗢 | | | |
| Project Navigator 🔥 Hierarchy 🔹 🔍 📮 🗗 🗙 | Compilation Report - EPT_4 | ICE6_AF_D1_Top | | | IP Catalog | ₽ ₽ × |
| Entity Instance | Table of Contents 📃 🗗 | Flow Summary | | | 2 | ×≡ |
| Cyclone IV F: EP4CE6E22C8 | Elow Summary | < <filter>></filter> | | | Y 🍰 Installed IP | ^ |
| > PFT 4CE6 AE D1 Top | Elow Settings | Flow Status | Flow Failed - Sun Aug 09 20:45:23 2020 | ^ | Y Project Directory | |
| | 📰 Flow Non-Default Global Set | Quartus Prime Version | 20.1.0 Build 711 06/05/2020 SJ Lite Edition | | No Selection Available | |
| | Flow Elapsed Time | Revision Name | EPT_4CE6_AF_D1_Top | | ✓ Library | |
| | Flow OS Summary | Top-level Entity Name | EPT_4CE6_AF_D1_Top | | > Basic Functions | |
| | Flow Log | Family | Cyclone IV E | | > DSP | |
| Tasks Compilation • = 4 6 × | 🔉 📒 Analysis & Synthesis | Device | EP4CE6E22C8 | | > Interface Protocols | |
| Task | Flow Messages | Timing Models | Final | | > Processors and Peripherals | |
| 🗙 👻 🕨 Compile Design | Flow Suppressed Messages | Total logic elements | N/A until Partition Merge | | > University Program | |
| X > Analysis & Synthesis | | Total registers | N/A until Partition Merge | | Search for Partner IP | ~ |
| < | < > | Total pins | N/A until Partition Merge | ~ | + Add | |
| | | 👼 Eind 💏 Find N | ext | | | |
| Type ID Message | | | | | | ^ |
| 12128 Elaborating entity | "endpoint_registers" for h | ierarchy "active_tr | ansfer_library:ACTIVE_TRANSFER_LIBRARY_I | ENST | endpoint_registers:ENDPOINT_F | REG: |
| 12128 Elaborating entity | "active trigger" for hiera | rchy "active trigge | ACTIVE TRIGGER INST | | | |
| 12128 Elaborating entity | "active_transfer" for hier | archy "active_trans | fer:ACTIVE_TRANSFER_INST_1" | | | |
| 12128 Elaborating entity | "accive_block for hierarc | hy "active_block:BLO | OCK_TRANSFER_INST" | | | |
| 12006 mode instance ACTI | <pre>VE_CONTROL_REG_INST Insta d messages file C:/lolly/C</pre> | intlates underlined en | Tity "active_control_register". Ensire | tha 6 AE | T required library paths are s | spe |
| Quartus Prime Analy | sis & Synthesis was unsucc | esstul. 1 error, 12 | warnings | | _010p.map.5m3g | |
| 293001 Quartus Prime Full | compilation was unsuccessf | ul. 3 errors, 12 wa | nings | | | |
| 8 × | | | | | | > |
| System (3) Processing (47) | | | | | | |
| 2 , | | | | | 11% 000 | 0:16 |

The error in this case is the missing file "active_control_register". Click on the Assignment menu, then select Settings, then select Files. Add the "active_control_register.v" file from the database.



| | General | Files | | | | | |
|---|-----------------------------------|--------------------|--------------------------|------------------------------------|-----------|-------------------------------|------------------|
| | Files | Select the | losign filos vou wont to | include in the project. Click Ar | | add all docign files in the p | roject |
| | Libraries | directory to | the project | o include in the project. Click At | IU All LO | add all design nies in the pi | roject |
| ~ | IP Settings | | s the project. | | | | |
| | IP Catalog Search Locations | <u>F</u> ile name: | | | | | <u>A</u> dd |
| | Design Templates | | | | | | |
| / | Operating Settings and Conditions | | | | | ~ | Add A <u>l</u> l |
| | Voltage | File Name | | Туре | Library | Design Entry/Synthesis 1 | Remove |
| | Temperature | src/ac | tive_control_register | Verilog Quartus Mapping File | | <none></none> | _ |
| / | Compilation Process Settings | src/ft | 245_state_machine.v | Verilog HDL File | | <none></none> | <u>U</u> p |
| | Incremental Compilation | src/ep | tWireOR.v | Verilog HDL File | | <none></none> | Down |
| / | EDA Tool Settings | src/EP | T_4CE6_AF_D1_Top.v | Verilog HDL File | | <none></none> | <u>D</u> own |
| | Design Entry/Synthesis | src/en | dpoint_registers.vqm | Verilog Quartus Mapping File | | <none></none> | Propertie |
| | Simulation | src/de | fine.v | Verilog HDL File | | <none></none> | |
| | Board-Level | src/ac | tive_trigger.vqm | Verilog Quartus Mapping File | | <none></none> | |
| / | Compiler Settings | src/ac | tive_transfer_library.v | Verilog HDL File | | <none></none> | |
| | VHDL Input | src/ac | tive_transfer.vqm | Verilog Quartus Mapping File | | <none></none> | |
| | Verilog HDL Input | src/ac | tive_block.vqm | Verilog Quartus Mapping File | | <none></none> | |
| | Default Parameters | | | | | | |
| | Timing Analyzer | | | | | | |
| | Assembler | | | | | | |
| | Design Assistant | | | | | | |
| | Signal Tap Logic Analyzer | | | | | | |
| | Logic Analyzer Interface | | | | | | |
| | Power Analyzer Settings | | | | | | |
| | SSN Analyzer | | | | | | |
| | | | | | | | |
| | | | | | | | |
| | | | | | | | |
| | | | | | | | |
| | | < | | | | | |
| | | | | | | | |

Click Ok then re-run the Compile process. Compilation progress is noted in bottom right corner.



| S Quartus Prime Lite Edition - C:/Users/nelso | /Documents/EPT_10CL | 016_AF_System_Demo/EPT_10CL016_AF_T2_Top/EPT_10CL016_AF | _T2_Top - EPT_10CL016_AF_T2_Top | - • × |
|---|--|---|--|--|
| Eile Edit View Project Assignments Pro | cessing Iools Wind | ow Help | | Search Intel FPGA |
| - 🗋 🚾 🖶 🤟 🗊 💼 つ 🐑 EPT_10CL | or 👻 🔟 🎸 🎸 🖉 | ◎ ▷ ≯ ½ ♀ ◎ ≛ ♥ 🖬 : ㅋ | | |
| Project Navigator 🔺 Hierarchy 👻 🔍 💷 👳 | Compilation Reg | ort - EPT 10CI 016 AF T2 Top X | | IP Catalog |
| Entity:Instance | Table of Contents III | | | |
| Cyclone 10 LP: 10CL016YE144C8G | Elow Summary | <pre>scale="block">scale="block">scale="block"</pre> | | ♥ ₩ Installed IP |
| + EPT_10CL016_AF_T2_Top * | Flow Settings Flow Non-Defa Flow Elapsed T Flow COS Summ Flow Log Analysis & Synt Flow Messages Flow Suppression | Flow Status In progress - Sat Feb 8 15:15:44 2025 Quartus Prime Version 23:1std.1 Build 993024 SC Lite Editid Revision Name EPT_10CL016_AF_1Z_Top Top-level Entity Name EPT_10CL016_AF_T2_Top Family Cyclone 10 LP | i n | Project Directory No Selection Available Library Basic Functions DSP Interface Protocols Memory Interfaces and Controllers Processors and Peripherals University Program Search for Partner IP |
| Tasks Compitation | | | | |
| 1ask | | | | |
| 98% Analysis & Synthesis | | | | |
| 0% Fitter (Place & Route) | | | | |
| 0% Assembler (Generate progr | | | | |
| 0% Timing Analysis | | | | |
| 0% 🕨 EDA Netlist Writer | | | | |
| ■ Edit Settings 👻 | | | | |
| • | • | | | * Add |
| All • All • <-Filter>> | | €€Eind ■Find Ne <u>x</u> t | | |
| Type ID Message | | | | |
| Bunning Quartus P Command: quartus P Command: quartus P 20030 Parallel compilat 12021 Found 1 design un 12021 Found 1 design un | rime Analysis & mapread_sett prs has not bee ion is enabled its, including its, including its, including its, including its, including its, including its, including its, including | Synthesis synthesis ungs_files=onwrite_settings_files=off EP i specified which may cause overloading on : und will use 4 of the 4 processors detected lentities, in source file /users/nelso/doc lentities, in source file /users/nelso/doc | r_10CL016_AF_T2_Top -C EPT_10CL016_AF_T2_TC shared machines. Set the global assignment uments/ept_10Cl016_af_system_demo/src/write uments/ept_10Cl016_af_system_demo/src/syrc/ uments/ept_10Cl016_af_system_demo/src/sypi_ uments/ept_10Cl016_af_system_demo/src/syster uments/ept_10Cl016_af_system_demo/src/syster uments/ept_10Cl016_af_system_demo/src/syster uments/ept_10Cl016_af_system_demo/src/syster | p NUM PARALLEL_PROCESSORS in your QS spi_master.v control_togic.v fifo.v face_master.v _segment_led_dsplay.v l_clock.v ed_control.v |
| System (2) Processing (105) | | | | 19% 00:00:13 |

After successful completion, the screen should look like the following:





At this point the project has been successfully compiled, synthesized and a programming file has been produce. See the next section on how to program the FPGA.

8 Configuring the FPGA

• Please Note: The CycloFlex Does Not Contain On Board Programmer. JTAG Programming and Configuration Flash Programming must be performed by external Programmer Purchased Separately.

Configuring the Cyclone 10 FPGA on the CycloFlex is the process of programming the compiled/synthesized user project into the FPGA. Once the FPGA is configured with the user project, the CycloFlex board is usable with the code. There are two methods to configure the Cyclone 10 FPGA

- Direct JTAG access
- On Board Configuration Flash chip



Direct JTAG access allows the Quartus Prime Lite software to program the object file directly into the FPGA using JTAG. This will configure the FPGA with the user project using volatile memory. If the power is removed from the Cyclone 10, the chip will lose its configuration.

On Board Configuration Flash chip programming allows the Quartus Prime Lite software to write to the CycloFlex Configuration Flash chip. The users compiled/synthesized project is loaded into the on board flash. Once the flash chip loading is complete, the CycloFlex will reset the FPGA. During the reset, the Cyclone 10 will load the contents of the Configuration Flash chip into the FPGA. If the FPGA is power cycled (Off/On), the chip will perform the loading from the flash chip.

The next two sections describe how to implement the JTAG direct and On Board Configuration Flash programming of the CycloFlex.

8.1 JTAG Direct Programming of the FPGA

Connect the CycloFlex to the PC via the USB-C connection, Connect a JTAG Blaster compatible programmer to the PC, connect the 10 pin cable from the Blaster to the JTAG connector of the CycloFlex board, open up Quartus Prime, open the programmer tool.



The CycloFlex includes programming switch that capable of six Dual Pole Single Throw connections. The JTAG/CONFIG SWITCH.



| <u>Q</u> | | | 015P1 LELL1 | DIS72 DISP3 (| |
|----------|--------------|--------------------|----------------|---------------|-------|
| 14 | IRC SENSOR | CONF_DOHE | | | SWITC |
| | I CONNECT | | | | |
| | | | | | _ |
| | J6 10 | la la u La la u | · · · · · | | |
| | JI 🗰 1 | J12 | SERIAL FLASH | | |

This switch is designed to allow the external Blaster Programmer to either program the Cyclone 10 chip directly using JTAG or program the Config Flash chip. Changing the position of the switch will allow the same Blaster to be used for either JTAG programming or Config Flash programming.



The JTAG Programming Path must have certain configuration pins of the Cyclone 10 in fixed positions (pulled up or pulled down) during programming. The following jumpers must be installed for correct programming of the Cyclone 10 chip using JTAG:

Page 141



- JMP7
- JMP6
- JMP5

A jumper is a two pin socket used to short two header pins together.



The jumper locations are:





The correct settings for JTAG Path Programming:





Once the jumpers and JTAG/Flash switch have been set, refer the section "Programming the CycloFlex" for instructions on how to use the Quartus Prime Lite software to program the Cyclone 10 chip.

Click on the Programmer button.


| Quartus Prime Lite Edition - C:/Jolly/Code_FPGA/EPT_10CL016_CB_System_Demo/EPT_10C | .016_CB_System_Demo/EPT_10CL016_AF_T2_Top/EPT_10CL016_AF_T2_Top - EPT_10CL016_AF_T2_Top |
|--|---|
| <u>File Edit View Project Assignments Processing Tools Window Help</u> | |
| | 2_Top → 2 ♦ ♦ ♦ 500 ► ★ ★ ♦ ♥ ₽ ₽ ₽ ₽ ₽ ₽ ₽ ₽ ₽ ₽ ₽ ₽ ₽ ₽ ₽ ₽ ₽ ₽ |
| | Table of Contents 🛛 🖗 🖉 Flow Summary |
| Entity:Instance Cyclone 10 LP: 10CL016YE144C8G P EPT_10CL016_AF_T2_Top Tasks Compilation Entity:Instance | Image: Second |
| Task | Total PLLs |
| ✓ ✓ ► Compile Design | |
| Analysis & Synthesis | |
| ✓ Fitter (Place & Route) | |
| Assembler (Generate programming files) | |
| ✓ ► Timing Analysis | • • • • • • • • • • • • • • • • • • • |
| | |
| | 66 Eind 66 Find Negt |
| Type ID Message | |
| 332140 No Hold paths to report 332140 No Recovery paths to report | |

The Programmer Window will open up with the programming file selected. Click on the Hardware Setup button in the upper left corner.



| Nrogrammer - [Chair | n1.cdf] | | | | | | | | | | - | | 3 | × |
|---|-------------------------------------|-------------------|----------|----------|-----------------------|--------|-----------------|---------|-----------------|--------|--------------|--------------|-------|------|
| <u>File E</u> dit <u>V</u> iew P <u>r</u> o | cessing <u>T</u> ools <u>W</u> indo | ow <u>H</u> elp | | | | | | | | Search | Intel F | PGA | | 9 |
| 🔔 Hardware Setup | EPT-JTAG-Blaster v1.0 | (64) [MBUSB-0] | | | Mode: JTA | s | | - I | Progress: | | | | | |
| Enable real-time ISF | to allow background pro | ogramming when av | ailable | | | | | | | | | | | |
| ▶ [™] Start | File | Device | Checksum | Usercode | Program/ Configure | Verify | Blank- Check | Examine | Security Bit | Erase | Reac ecks | ISP CLAMP | 'S Fi | (P F |
| Stop | | | | | | | | | | | | | | |
| Huto Detect | | | | | | | | | | | | | | |
| X Delete | | | | | | | | | | | | | | |
| Ma Add File | | | | | | | | | | | | | | • |
| Change File | | | | | | | | | | | | | | |
| Save File | | | | | | | | | | | | | | |
| Add Device | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | |
| + Down | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | |

The Hardware Setup Window will open. In the "Available hardware items", double click on "EPT-JTAG-Blaster v1.0b (64)".



| Hardware Settings JTAC | 5 Settings | | | | |
|--|---------------------------|-----------------------------|----------------------------------|-----------------------|----|
| Select a programming hard hardware setup applies only | vare setup to the curr | to use when rent program | programming devi omer window. | ces. This programming | |
| Currently selected hardware | EPT-JT | AG-Blaster v | /1.0 (64) [MBUSB-0] | | ¥ |
| Hardware frequency: | | | | | H: |
| Available hardware items | | | | | |
| Hardware | _ | Server | Port | Add Hardware | 1 |
| EPT-JTAG-Blaster v1.0 (6 | 54) | Lotal | MBUSB-0 | Remove Hardware | j |
| | | | | | |
| | | | | | |
| | | | | | |
| | | | | | |
| | | | | | |
| | | | | | |

If you successfully double clicked, the "Currently selected hardware:" dropdown box will show the "EPT-JTAG-Blaster v1.0b (64)".



| Hardware Settings JTAG Setting | s | | |
|---|-----------------------------------|------------------------------------|-----------------------|
| Select a programming hardware set hardware setup applies only to the c | up to use when current program | programming device omer window. | ces. This programming |
| Currently selected hardware. | -JTAG-Blaster | /1.0 (64) [MBUSB-0] | >` |
| Hardware frequency: | | | н |
| Available hardware items | | | |
| Hardware | Server | Port | Add Hardware |
| EPT-JTAG-Blaster v1.0 (64) | Local | MBUSB-0 | Remove Hardware |
| | | | |
| | | | |
| | | | |
| | | | |
| | | | |
| | | | |

Click on the "Add File" button



| EPT-JTAG-Blaster v1.0 (| 64) [MBUSB-0] | | | | | | | | | | | |
|-------------------------|------------------|-------------|----------------------|-------------------------------|---|--|---|--|---|---|--|--|
| to allow background pro | gramming when av | ailable | | Mode: JTAC | 5 | | ₹ P | rogress: | | | | |
| File | Device | Checksum | Usercode | Program/ Configure | Verify | Blank- Check | Examine | Security Bit | Erase | Reac ecks | ISP CLAMP | 'S Fi (P F |
| | | | | | | | | | | | | |
| | | | | | | | | | | | | Þ |
| | | | | | | | | | | | | |
| | | | | | | | | | | | | |
| | | | | | | | | | | | | |
| | | | | | | | | | | | | |
| | File | File Device | File Device Checksum | File Device Checksum Usercode | File Device Checksum Usercode Program/ Configure | File Device Checksum Usercode Program/ Verity Configure | File Device Checksum Usercode Program/ Verity Blank- Configure Check | File Device Checksum Usercode Program/ Venty Blank- Examine Configure Check | File Device Checksum Usercode Program/ Configure Verify Blank- Check Examine Security | File Device Checksum Usercode Program/ Configure Verify Blank- Check Examine Security Enase | File Device Checksum Usercode Program/ Verity Blank- Examine Security Erase Read Configure Check Bit icks | File Device Checksum Usercode Program/ Configure Verify Check Blank- Bit Examine Bit Erase scks CLAMP |



| Nelect Programming File | | | | | | | | × |
|--|--|----------------------------|----------------------------|------------------------|----------------------|-----|--------------|---|
| Look in: C:\Jolly\Code_FPGA\EPT_10 | OCL016_CB_System_Demo\EPT_10CL016_CB_9 | System_Demo\EPT_10CL016_AF | _T2_Top | - (| 0 | 0 🗭 | | |
| My Computer | Name | ▲ Size | Туре | Date Modifi | ed | | | |
| nelso | db incremental db | | File Folder File Folder | 1/26/2025 10/12/202 | 6:26 PM 2 8:58 PM | | | |
| | output_files | | File Folder | 1/26/2025 | 6:24 PM | | | |
| | | | | | | | | |
| | | | | | | | | |
| | | | | | | | | |
| | 4 | | | | | | | Þ |
| File <u>n</u> ame: | | | | | | | <u>O</u> pen | |
| Files of type: Programming Files (*.sof *.pof *. | jam *.jbc *.ekp *.jic) | | | | | • | Cance | L |

At the Browse window, double click on the output files folder.

| Nelect Programming File | | | | | | × |
|--|--|---|----------------------------------|-------------------------------------|---|---------------------|
| Look in: C:\Jolly\Code_FPGA\EPT | _10CL016_CB_System_Demo\EPT_10CL016_CB_System_De | emo\EPT_10CL016_AF_T2_Top\output_files | Ŧ | 00 | 0 | : = |
| My Computer | Name | ▲ Size Type | Date Mod | fied | | |
| nelso nelso | EPT_10CL016_AF_T2_Top.sof | 485.31 KiB sof File 512.20 KiB pof File 512.20 KiB pof File | 1/26/202 1/18/202 4/9/2021 | 5 6:24 PM 5 11:12 PI 10:42 AM | м | |
| File <u>n</u> ame: Files of type: Programming Files (*.sof *.po | f*.jam *.jbc *.ekp *.jic) | | | | | ▶ Open Cancel |

Double click on the "EPT_10CL016_AF_T2_Top.sof" file. Click the Open button in the lower right corner.



| Programmer - [Chain <u>File</u> <u>Edit</u> <u>View</u> Pro | n1.cdf]* ocessing <u>T</u> ools <u>W</u> indow <u>H</u> elp | | | | | | Searc | — | |
|--|--|--------------|------------|----------|----------------|----------|--------|---------|------------|
| Aardware Setup | EPT-JTAG-Blaster v1.0 (64) [MBUSB-0] | | Mode: JTAG | i | • | Progress | | | |
| Enable real-time ISF | P to allow background programming when available File | Device | Checksum | Usercode | Program/ | Verify | Blank- | Examine | Security f |
| Stop C | C:/Jolly/Code_FPGA/EPT_10CL016_CB_System_Dem | 10CL016YE144 | 001796D0 | 001796D0 | Configure V | | Check | | Bit |
| Auto Detect | | | | | | | | | |
| Add File | 4 | | | | | | | | Þ |
| Save File | | | | | | | | | |
| 1 th Up | TDI (me) | | | | | | | | |
| J [™] Down | TPORL016YE144 | | | | | | | | |
| | | | | | | | | | |
| | | | | | | | | | |
| | | | | | | | | | |

Next, selet the checkbox under the "Program/Configure" of the Programmer Tool.



| Nrogrammer - [Chai | n1.cdf]* | | | | | | | - | o x |
|---|---|--------------|------------|----------|-----------------------|-----------|-----------------|---------------|-----------------|
| <u>File E</u> dit <u>V</u> iew P <u>r</u> o | cessing <u>T</u> ools <u>W</u> indow <u>H</u> elp | | | | | | Searc | ch Intel FPGA | 6 |
| Aardware Setup | EPT-JTAG-Blaster v1.0 (64) [MBUSB-0] | | Mode: JTAG | ; | • | Progress: | | | |
| Enable real-time IS | to allow background programming when available | | | | | | | | |
| ▶ [™] Start | File | Device | Checksum | Usercode | Program/ Configure | Verify | Blank- Check | Examine | Security Bit |
| Stop | :/Jolly/Code_FPGA/EPT_10CL016_CB_System_Dem | 10CL016YE144 | 001796D0 | 001796D0 | V | | | | |
| 💏 Auto Detect | | | | | | | | | |
| X Delete | | | | | | | | | |
| Add File | | | | | | | | | |
| Change File | t | | | | | | | | |
| Save File | | | | | | | | | |
| Add Device | | | | | | | | | |
| | HUELUIDYEI44 | | | | | | | | |
| | | | | | | | | | |
| | | | | | | | | | |
| | | | | | | | | | |
| | | | | | | | | | |
| | | | | | | | | | |

Click on the Start button to to start programming the FPGA. The Progress bar will indicate the progress of programming.



| Programmer - [Ch File Edit View F | nain1.cdf]* Processing Tools Window Help | | | | | | | - | |
|--------------------------------------|--|--------------|------------|----------|-----------------------|-----------|-----------------|---------|-------------------|
| Hardware Setup. | EPT-JTAG-Blaster v1.0 (64) [MBUSB-0] | | Mode: JTAG | | Ŧ | Progress: | Searc | 0% | |
| Enable real-time | ISP to allow background programming when available | 1 | | | | | | | |
| ▶ [™] Start | File | Device | Checksum | Usercode | Program/ Configure | Verify | Blank- Check | Examine | Security I Bit |
| ■ [™] Stop | C:/Jolly/Code_FPGA/EPT_10CL016_CB_System_Dem | 10CL016YE144 | 001796D0 | 001796D0 | \checkmark | | | | |
| Auto Detect | | | | | | | | | |
| X Delete | | | | | | | | | |
| Add File | | | | | | | | | |
| Change File | 4 | | | | | | | | • |
| Save File | | | | | | | | | |
| Add Device | | | | | | | | | |
| t [™] up | | | | | | | | | |
| J [™] Down | | | | | | | | | |
| | 1202L016YE144 | | | | | | | | |
| | | | | | | | | | |
| | | | | | | | | | |
| | | | | | | | | | |
| | | | | | | | | | |
| | | | | | | | | | |

When the programming is complete, the Progress bar will indicate success.



| Nrogrammer - [Chair | n1.cdf]* | | | | | | | - | |
|---|---|--------------|------------|----------|-----------------------|----------|-----------------|---------------|-----------------|
| <u>F</u> ile <u>E</u> dit <u>V</u> iew P <u>r</u> o | cessing <u>T</u> ools <u>W</u> indow <u>H</u> elp | | | | | | Sear | ch Intel FPGA | 6 |
| Aardware Setup | EPT-JTAG-Blaster v1.0 (64) [MBUSB-0] | | Mode: JTAG | i | • | Progress | | 100% (Succe | ssful) |
| Enable real-time ISF | to allow background programming when available | | | | | | | | |
| ▶ [™] Start | File | Device | Checksum | Usercode | Program/ Configure | Verify | Blank- Check | Examine | Security Bit |
| Muto Detect Muto Detect Model File | :/Jolly/Code_FPGA/EPT_10CL016_CB_System_Dem | 10CL016YE144 | 001796D0 | 001796D0 | V | | | | |
| Change File | TDI | | | | | | | | |

If the Programming window indicates that the "Progress:" is 100% (Successful), the FPGA has been programmed directly though JTAG. The CycloFlex is now ready for use or debugging code.

If the power is cycled (Off/On), the FPGA will lose the *.sof file and the FPGA becomes a blank chip. Repeat the previous steps to program the user project into the FPGA directly with the JTAG.



8.2 Configuration Flash Programming of the FPGA

The Cyclone 10 FPGA requires configuration before it can be used to perform the functions of the user code. The CycloFlex board includes a 4Mbit Configuration Flash chip that is designed to store the user code. Then, when the power is cycled (On/Off), the FPGA will read the contents of the Configuration Flash and set up the functionality of the user code within the chip. The user will program a *.pof file into the flash chip using Quartus.

The board requires power from either Barrel Connector or USB-C Connector. Then connect the Blaster.



The CycloFlex includes a programming switch that is capable of six Dual Pole Single Throw connections. The JTAG/CONFIG SWITCH.



| | | DISPI DI LILLIL | 572 DISP3 |) JTAG/CO |
|---------|-----|--------------------|-----------|--------------|
| | | | | |
| | | | | |
| | | PROG | | |
| J6 10 | | | | |
| JI 10 1 | J12 | SERIAL FLASH | JTAG | |

This switch is designed to allow the external Blaster Programmer to either program the Cyclone 10 chip directly using JTAG or program the Config Flash chip. Changing the position of the switch will allow the same Blaster to be used for either JTAG programming or Config Flash programming.



The JTAG Programming Path must have certain configuration pins of the Cyclone 10 in fixed positions (pulled up or pulled down) during programming. The following jumpers must be installed for correct programming of the Configuration Flash:



- JMP7
- JMP6
- JMP5

A jumper is a two pin socket used to short two header pins together.



The jumper locations are:





The CycloFlex should be configure with the following:





Once the jumpers and JTAG/Flash switch have been set, refer the section "Programming the CycloFlex" for instructions on how to use the Quartus Prime Lite software to program the Cyclone 10 chip.

Click on the Programmer button.



| Quartus Prime Lite Edition - C:/Jolly/Code_FPGA/EPT_10CL016_CB_System_Demo/EPT_10C | .016_CB_System_Demo/EPT_10CL016_AF_T2_Top/EPT_10CL016_AF_T2_Top - EPT_10CL016_AF_T2_Top |
|--|---|
| <u>File Edit View Project Assignments Processing Tools Window Help</u> | |
| | 2_Top → 2 ♦ ♦ ♦ 500 ► ★ ★ ♦ ♥ ₽ ₽ ₽ ₽ ₽ ₽ ₽ ₽ ₽ ₽ ₽ ₽ ₽ ₽ ₽ ₽ ₽ ₽ |
| | Table of Contents 🛛 🖗 🖉 Flow Summary |
| Entity:Instance Cyclone 10 LP: 10CL016YE144C8G P EPT_10CL016_AF_T2_Top Tasks Compilation Entity:Instance | Image: Second |
| Task | Total PLLs |
| ✓ ✓ ► Compile Design | |
| Analysis & Synthesis | |
| ✓ Fitter (Place & Route) | |
| Assembler (Generate programming files) | |
| ✓ ► Timing Analysis | • • • • • • • • • • • • • • • • • • • |
| | |
| | 66 Eind 66 Find Negt |
| Type ID Message | |
| 332140 No Hold paths to report 332140 No Recovery paths to report | |

The Programmer Window will open up with the programming file selected. Click on the Hardware Setup button in the upper left corner.



| Nrogrammer - [Chair | n1.cdf] | | | | | | | | | | - | | 3 | × |
|---|-------------------------------------|-------------------|----------|----------|-----------------------|--------|-----------------|---------|-----------------|--------|--------------|--------------|-------|------|
| <u>File E</u> dit <u>V</u> iew P <u>r</u> o | cessing <u>T</u> ools <u>W</u> indo | ow <u>H</u> elp | | | | | | | | Search | Intel F | PGA | | 9 |
| 🔔 Hardware Setup | EPT-JTAG-Blaster v1.0 | (64) [MBUSB-0] | | | Mode: JTA | s | | - I | Progress: | | | | | |
| Enable real-time ISF | to allow background pro | ogramming when av | ailable | | | | | | | | | | | |
| ▶ [™] Start | File | Device | Checksum | Usercode | Program/ Configure | Verify | Blank- Check | Examine | Security Bit | Erase | Reac ecks | ISP CLAMP | 'S Fi | (P F |
| Stop | | | | | | | | | | | | | | |
| Huto Detect | | | | | | | | | | | | | | |
| X Delete | | | | | | | | | | | | | | |
| Ma Add File | | | | | | | | | | | | | | • |
| Change File | | | | | | | | | | | | | | |
| Save File | | | | | | | | | | | | | | |
| Add Device | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | |
| + Down | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | |

The Hardware Setup Window will open. In the "Available hardware items", double click on "EPT-JTAG-Blaster v1.0b (64)".



| Hardware Settings JTAG S | ettings | | |
|---|---|-------------------------------------|-----------------------|
| Select a programming hardwa hardware setup applies only to | re setup to use when the current program | n programming devie nmer window. | ces. This programming |
| Currently selected hardware: | EPT-JTAG-Blaster | v1.0 (64) [MBUSB-0] | Ŧ |
| Hardware frequency: | | | н |
| Available hardware items | | | |
| Hardware | Server | Port | Add Hardware |
| EPT-JTAG-Blaster v1.0 (64) | Lo al | MBUSB-0 | Remove Hardware |
| | | | |
| | | | |
| | | | |
| | | | |
| | | | |

If you successfully double clicked, the "Currently selected hardware:" dropdown box will show the "EPT-JTAG-Blaster v1.0b (64)".



| Hardware Settings JTAG Setting | s | | |
|---|-----------------------------------|---------------------------------------|-----------------------|
| Select a programming hardware set hardware setup applies only to the c | up to use wher current program | n programming device Inmer window. | ces. This programming |
| Currently selected hardware. EPT Hardware frequency: Available hardware items | -JTAG-Blaster | v1.0 (64) [MBUSB-0] | |
| Hardware | Server | Port | Add Hardware |
| EPT-JTAG-Blaster v1.0 (64) | Local | MBUSB-0 | Remove Hardware |
| | | | |
| | | | |
| | | | |

Click on the "Mode:" drop down box. Select the "Active Serial Programming" option.



| 👋 Programmer - C:/ | Jolly/Code_FPGA/EPT_4CE | 5_AF_Data_Collecto | or_2/EPT_4CE6_AF | -D1_Top - EPT_4 | CE6_AF_D1_Top | o - [EP | - | o x |
|----------------------|----------------------------|--------------------|-----------------------------------|-----------------|-----------------------|---------|-----------------|---------|
| File Edit View | Processing Tools Win | dow Help | | | | Sea | rch altera.c | om 🌖 |
| 🚖 Hardware Setup. | Blaster v1.6b (64) [MBl | JSB-0] Mode: | JTAG | • | Progress: | | | |
| Enable real-time I | SP to allow background pro | ogramming when a | JTAG In-Socket Prog | gramming | | | | |
| ► [₩] Start | File | Device | Passive Serial Active Serial P | rogramming | Program/ Configure | Verify | Blank- Check | Examine |
| Stop | output_files/EPT_4CE6 | EP4CE6E22 | 000C47F6 | 000C47F6 | \checkmark | | | |
| 💏 Auto Detect | | | | | | | | |
| 🗙 Delete | | | | | | | | |
| 💾 Add File | | | | | | | | |
| Change File | < | | | | | | | > |
| Save File | | | | | | | | |
| 📌 Add Device | (intel) | : | | | | | | |
| 1 Шир | | | | | | | | |
| ^{‡™} Down | | | | | | | | |
| | EP4CE6E2 | 22 | | | | | | |
| | + | | | | | | | |
| | | | | | | | | |
| | | | | | | | | |
| | | | | | | | | |

Click on the "Add File" button



| Programmer - [Chai <u>File Edit View Pro</u> | n1.cdf] ocessing <u>T</u> ools <u>W</u> indo | ow <u>H</u> elp | | | | | | | | Search I | ntel F | PGA | | × |
|---|---|------------------|----------|----------|-----------------------|--------|-----------------|---------|-----------------|----------|---------------|--------------|-------|------|
| Hardware Setup | EPT-JTAG-Blaster v1.0 | (64) [MBUSB-0] | | | Mode: JTA | G | | • F | Progress: | | | | | |
| Enable real-time ISP | P to allow background pro | ogramming when a | Checksum | Usercode | Program/ Configure | Verify | Blank- Check | Examine | Security Bit | Erase | Reac ecksi | ISP CLAMP | 'S Fi | (P F |
| Auto Detect | | | | | | | | | | | | | | |
| Add File | (| | | | | | | | | | | | | • |
| Save File | | | | | | | | | | | | | | |
| 1 ¹⁰ Up | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | |

In the DVD project, navigate to the C:\CycloFlex_FPGA_SYSTEM_PROJECT_x.x_DVD (The "x.x" is the latest available version of the project DVD).



| $\leftarrow \rightarrow \uparrow \bigcirc \square \rightarrow \text{This PC} \Rightarrow \text{Windows (C:)} \Rightarrow \text{Jolly} \Rightarrow \text{Poly}$ | roducts > Earth People Technology | > CYCLOFLEX_FPGA | SYSTEM_PROJECT | [_1.0_DVD > | | | |
|---|--|-------------------|----------------|-------------|--|--|--|
| ⊕ New ~ | | | | | | | |
| ✓ ► Earth People Technology | Name | Date modified | Туре | Size | | | |
| BEEPROLOGIC_CPLD_DEV_SYS_PROJECT_1.0_DVD | Documentation | 1/22/2025 9:22 PM | File folder | | | | |
| > CYCLOFLEX_FPGA_SYSTEM_PROJECT_1.0_DVD | Drivers | 1/22/2025 9:22 PM | File folder | | | | |
| DSO_100M_DEV_SYS_PROJECT_2.8_DVD | Projects_ActiveHost | 1/22/2025 9:33 PM | File folder | | | | |
| > DUEPROLOGIC USB FPGA PROJECT 5.0 DVD | Projects_HDL | 1/22/2025 9:34 PM | File folder | | | | |
| > EPT I2C Project CD | Quartus_24.1_Prime | 1/22/2025 9:22 PM | File folder | | | | |
| | Tutorials | 1/22/2025 9:23 PM | File folder | | | | |
| > EPI Projects Folders | | | | | | | |
| ESP32_DJ_SNACK_PACK_PROJECT_4.0_DVD | > Control Cont | | | | | | |
| MAXPROLOGIC_FPGA_PROJECT_4.0_DVD | > MAXPROLOGIC_FPGA_PROJECT_4.0_DVD | | | | | | |

Double Click ont eh Projects_HDL folder

| Nelect Prog | ramming File | | × |
|--------------------|---|---|---|
| Look in: | C:\Jolly\Products\Earth People Technology\CYCLO | FLEX_FPGA_SYSTEM_PROJECT_1.0_DVD | - 🗘 🗘 🖓 🗰 🗏 |
| My Comp | uter Name Documentation Drivers Projects_ActiveHost Projects_HDL Quartus_24:1_Prime Tutorials | Size Type File Folder File Folder File Folder File Folder File Folder File Folder | Date Modified 1/22/2025 9:22 PM 1/22/2025 9:22 PM 1/22/2025 9:33 PM 1/22/2025 9:34 PM 1/22/2025 9:22 PM 1/22/2025 9:23 PM |
| | | | • |
| File <u>n</u> ame: | | | <u>O</u> pen |
| Files of type: | POF Files (*.pof) | | ▼ Cancel |

Double Click on the EPT_10CL016_CB_System_Demo Folder



| Nelect Prog | amming File | × |
|--------------------|--|--------------|
| Look in: | 🗎 C:\Jolly\Products\Earth People Technology\CYCLOFLEX_FPGA_SYSTEM_PROJECT_1.0_DVD\Projects_HDL 🛛 🔻 🤤 📀 🚱 🞉 🗄 | : 🔳 |
| 💻 My Comp | er Name Size Type Date Modified | |
| nelso | File Folder 1/22/2025 9:34 PM | |
| | 4 | Þ |
| File <u>n</u> ame: | | <u>O</u> pen |
| Files of type: | POF Files (*.pof) | Cancel |

Double Click on the EPT_10CL016_AF_T2_Top Folder



| Nelect Prog | ramming File | 2 | | | | × |
|--------------------|--------------|---|-----------------------------|--------------------|-------------------|--------------|
| Look in: | C:\Jolly\ | Products\Earth People Technology\CYCLO1.0 | _DVD\Projects_HDL\EPT_10CLC | 016_CB_System_Demo | • • • • • • • • | :: 🔳 |
| 💻 My Compu | uter | Name | ▲ Size | Type | Date Modified | |
| nelso | | Altera | | File Folder | 1/22/2025 9:34 PM | |
| netso | | EPT_10CL016_AF_T2_Top | | File Folder | 1/22/2025 9:34 PM | |
| | | ModelSim | | File Folder | 1/22/2025 9:34 PM | |
| | | iii sim | | File Folder | 1/22/2025 9:34 PM | |
| | | src src | | File Folder | 1/22/2025 9:34 PM | |
| | | est test | | File Folder | 1/22/2025 9:34 PM | |
| | | Testbench | | File Folder | 1/22/2025 9:34 PM | |
| | | | | | | |
| | | | | | | |
| | | | | | | |
| | | | | | | |
| | | | | | | |
| | | | | | | |
| | | | | | | |
| | | | | | | |
| | | | | | | |
| | | | | | | |
| | | • | | | | Þ |
| File <u>n</u> ame: | | | | | | <u>O</u> pen |
| Files of type: | POF Files (* | *.pof) | | | - | Cancel |

Double Click on the output_files Folder

| Nelect Programming File | | | | | · | | × |
|---|--|-------------------------------|---|--|--|-------------|-----|
| Look in: C:\Jolly\Code_FPGA\E | PT_10CL016_CB_System_Demo\EPT_10CL016_CB | B_System_Demo\EPT_10CL016_AF_ | Г2_Тор | • | 0 0 0 | i | |
| My Computer | Name db incremental db output_files | ▲ Size | Type File Folder File Folder File Folder | Date Modi 1/26/202 10/12/202 1/26/202 | fied 5 6:26 PM 22 8:58 PM 5 6:24 PM | | |
| | 4 | | | | | | Þ |
| File <u>n</u> ame: | | | | | | <u>O</u> pe | en |
| Files of type: Programming Files (*.sof * | .pof *.jam *.jbc *.ekp *.jic) | | | | | • Can | cel |



Double click on the "EPT_10CL016_AF_T2.pof" file.

| Nelect Program | ming File | | × |
|--------------------|---|--|---|
| Look in: | C:\Jolly\Products\Earth People Technology\CYCLOFB_Sys | stem_Demo\EPT_10CL016_AF_T2_Top\output_files | - 🔾 🖓 🖓 🗮 🗏 |
| 💻 My Computer | Name | ▲ Size Type | Date Modified |
| nelso | Output_file.pof | 512.20 KiB pof File 512.20 KiB pof File | 1/18/2025 11:12 PM 4/9/2021 10:42 AM |
| File name: | | | • |
| File <u>n</u> ame: | | | <u>O</u> pen |
| Files of type: PC |)F Files (*.pof) | | ▼ Cancel |

Double click on the "EPT_10CL016_AF_T2.pof" file. Click the Open button in the lower right corner.

Select the EPCS1 under "Device".



| 👋 Programmer - C: | /Jolly/Code_FPGA/EPT_4CE | 6_AF_Data_Collector | _2/EPT_4CE6_AF | D1_Top - EPT_4 | CE6_AF_D1_To | p - [EP | - | o x |
|--|---|---------------------|-------------------|----------------|-----------------------|---------|-----------------|---------|
| <u>F</u> ile <u>E</u> dit <u>V</u> iew | P <u>r</u> ocessing <u>T</u> ools <u>W</u> ir | idow <u>H</u> elp | | | | Sea | rch altera.c | om 🌖 |
| 🚖 Hardware Setup | Blaster v1.6b (64) [MB | USB-0] Mode: | Active Serial Pro | ogramming 🔻 | Progress: | | | |
| Enable real-time | ISP to allow background p | ogramming when av | ailable | | | | | |
| ▶ ⁹ Start | File | Device | Checksum | Usercode | Program/ Configure | Verify | Blank- Check | Examine |
| ■ [™] Stop | /EPT_4CE6_AF_Data | EPCS1 | 007971BD | 0000000 | | | | |
| Auto Detect | | <u> </u> | | | | | | |
| 🗙 Delete | | | | | | | | |
| Add File | | | | | | | | |
| 隆 Change File | < | | | | | | | > |
| Save File | | | | | | | | |
| Add Device | (inter) | | | | | | | |
| 1 ^ካ Up | ASDI | | | | | | | |
| ‡ [%] bown | | | | | | | | |
| | EPCS1 | | | | | | | |
| | • | | | | | | | |
| | | | | | | | | |
| | | | | | | | | |
| | | | | | | | | |

Next, selet the checkbox under the "Program/Configure" of the Programmer Tool.



| 👋 Programmer - C:/ | /Jolly/Code_FPGA/EPT_4CE6 | 5_AF_Data_Collector | _2/EPT_4CE6_AF_ | D1_Top - EPT_4 | CE6_AF_D1_To | p - [EP | - | |
|--|--|---------------------|-------------------|----------------|-----------------------|---------|-----------------|---------|
| <u>F</u> ile <u>E</u> dit <u>V</u> iew | P <u>r</u> ocessing <u>T</u> ools <u>W</u> ine | dow <u>H</u> elp | | | | Sea | rch altera.c | om 🌖 |
| 🚖 Hardware Setup. | Blaster v1.6b (64) [MBU | JSB-0] Mode: | Active Serial Pro | ogramming 🔻 | Progress: | | | |
| Enable real-time | ISP to allow background pro | ogramming when av | ailable | | | | | |
| ▶ [™] Start | File | Device | Checksum | Usercode | Program/ configure | Verify | Blank- Check | Examine |
| ■ [™] Stop | /EPT_4CE6_AF_Data | EPCS1 | 007971BD | 00000000 | |) 🗆 | | |
| Auto Detect | | | | | \smile | | | |
| 🗙 Delete | | | | | | | | |
| Add File | | | | | | | | |
| Change File | < | | | | | | | > |
| Save File | | | | | | | | |
| Add Device | | | | | | | | |
| 1 ¹⁰ Up | ASDI | | | | | | | |
| ^{‡™} Down | | | | | | | | |
| | EPCS1 DATA | | | | | | | |
| | • | | | | | | | |
| | | | | | | | | |
| | | | | | | | | |
| | | | | | | | | |



Move the JTAG switch to the "Flash" position



Add JMP7 to Pins 2& 3.



Click on the Start button to to start programming the FPGA. The Progress bar will indicate the progress of programming.



| 👋 Programmer - C:, | /Jolly/Code_FPGA/EPT_4CE | 6_AF_Data_Collector_2 | 2/EPT_4CE6_AF_ | D1_Top - EPT_40 | CE6_AF_D1_Top | o - [EP | - | |
|---|---|-----------------------|-------------------|-----------------|-----------------------|---------|-----------------|---------|
| <u>F</u> ile <u>E</u> dit <u>V</u> iew | P <u>r</u> ocessing <u>T</u> ools <u>W</u> ir | idow <u>H</u> elp | | | | Sea | rch altera.c | om 🌀 |
| 📥 Hardware Setup | Blaster v1.6b (64) [MB | USB-0] Mode: | Active Serial Pro | ogramming 🔻 | Progress: | | | |
| Enable real-time | ISP to allow background p | ogramming when ava | iilable | | | | | |
| Start | File | Device | Checksum | Usercode | Program/ Configure | Verify | Blank- Check | Examine |
| Stop | /EPT_4CE6_AF_Data | EPCS1 | 007971BD | 0000000 | | | | |
| Auto Detect | | | | | | | | |
| Add File | | | | | | | | |
| 隆 Change File | < | | | | | | | > |
| Save File | | | | | | | | |
| /ີ Add Device ໃ ^ນ ີມ Up ມ ^າ ີມ Down | ASDI EPCS1 | | | | | | | |
| | | | | | | | | |

The programming of the CycloFlex will start and you can check the progress in the "Progress" Bar.





When the programming is complete, the Progress bar will indicate success.





Once the Quartus Programmer has completed, move the JTAG Switch into the "JTAG" Position.





Go back to the EPT CycloFlex Production Test Software folder. Double click on the "EPT_System_Demo.exe" file





The CycloFlex Production Test software will open

| | LED LOT I mm a 1 mm a 1 mm as | | IFR R I R I F T I | | | |
|---|--|-------------------------------|---|--|--|--|
| | LED 1 LED 2 LED 31 | LED 4 LED 5 LED 6 LED 7 LED 8 | LED Display Production Test | Test | | |
| Open Close | On On On | On On On On O | A ~ A ~ A ~ | Shift Right | | |
| | Shift Left Shift R | ight Count Up Count Dwn | | Blink | | |
| Transfer Production Test | | PushButton | Diap 1 Diap 2 Diap 3 | Stop | | |
| Send Byte Test: | Receive Byte | Controls Suitabase | RGB LED Production Test | | | |
| Start | | SWILCHES | | Test | | |
| | | | Red Blue Green Reset | | | |
| | | Rst | On On On Bet | | | |
| | | | | | | |
| | | 35 | | | | |
| GPIO Production Test | | | | | | |
| التراشات | | | | | | |
| | · · · · · · · | · · · · · · · · | | | | |
| | and the second | a first state of the | | | | |
| | | | OISPI DISP2 DISP: | 1 | | |
| and the second se | A REAL PROPERTY AND INC. | | อยีเป็นนี้นั้นของอาธิออ อ | | | |
| | | | | | | |
| X | | | 1 minimum | 3 | | |
| Stat Test | STATES IN LOSS | 1 | | | | |
| 8.000 | a a a le Ha ME | | | | | |
| ando | | CONF DONE | 10 | | | |
| | IC. IRC SENSOR | | and the second second second | | | |
| O Infinite | | | | | | |
| | | | COLODED STORE | | | |
| and the second se | CONNECT | | LED DIRECT | | | |
| | Dep dal d Bet San | | | | | |
| O Single | | | | | | |
| | | | 1 第一 1 1 | | | |
| | p | Cycron | a'10 🔮 🔨 🚛 📥 🛶 | | | |
| | EARTHPEOPLE | | JING JING | and the second sec | | |
| | a crucior | | PROGRAMING | | | |
| | | | 1 2 111 | | | |
| - Detty | | 1 1 1 | and the reason | (C | | |
| a Har | | | | and the second se | | |
| | til and an and | | | | | |
| | | A 1 27 00 00 1 | | · · · | | |
| the de | | | 1 | | | |
| The second second | | | 100 | 2 | | |
| | | | CL PROFILE | · · · | | |
| 2.0 | | | - 1 1 | ••• | | |
| II | | | | | | |
| | | | | | | |
| | | | | | | |
| | | | | | | |
| الشالشالشا | فالفلغالغالف | | | | | |
| | | | | | | |
| | | | | | | |
| | | | | | | |



Click on the Drop Down Box below the "EPT_System_Demo" text.





Select the "CycloFlex Board 0"

| | LED Cor | LED 1 LED 2 | LED 3LED | 4 LED 5 LE | ED 6 LED 7 LED 8 | LED (|
|---|---------|-------------|-------------|------------|------------------------------------|-------|
| cloFlex Board 0 | | On On | On On | On | On On O | A |
| | | Shift Left | Shift Right | Count Up | Count Dwn | |
| ransfer Production Test Send Byte Test: Start | Rece | ive Byte | | | PushButton Controls Switches | RGB |
| | | | * | | Fist | Rei |
| PIO Production Test | | | R# | | | |
| | | - | | - | - | 1 |
| | | | | | | |



Click the "Open" button

| iyolo Flex Board 0 🗸 🗸 | LED Control LED 1 LED 2 | LED 3 LED 4 LED 5 L | ED 6 LED 7 LED 8 | LED Display Pr |
|--|----------------------------|----------------------|------------------------------------|----------------|
| Open Close | On On | On On On | On On O | A ~ |
| | Shift Left | Shift Right Count Up | Count Dwn | Concerned in |
| Transfer Production Test Send Byte Test: Start | Receive Byte | | PushButton Controls Switches | RGB LED Pro |
| | | | 1000 | Red Blue |
| | | v | Fiat | On On |
| | 5 | Rat | | |
| GPIO Production Test | | | | |
| | بالبالبالبالب | لعلمالماله | 그그그그 | |
| <u></u> | بالبالباليات | الالكالكال | لعاصاصات | |
| | | 100 | | DIS |
| X | | | | |
| Start Test | THE TRACE IS A | | | 1000 |

Page 180


Ensure that the "Heartbeat" function is displayed on the Green User LEDs (repeating sweep of the LEDs)



At this point, the CycloFlex is programmed and ready for use.

8.3 Creating a *.pof File for Configuration Flash

In the previous section, it was outlined how to program the Configuration Flash on the CycloFlex using Quartus Prime Lite. The instructions used the *.pof file that was created by EPT for the EPT_System_Demo project. The *.pof must be created for each project the user creates. This section provides instructions on how to create a *.pof file for your project.

Generation of *.pof file from *.sof file for Altera FPGA What is *.sof & *.pof file?

*.sof is SRAM Object File & *.pof is Programming Object File. Both files are used to configure FPGA.

FPGA contains SRAM. It holds the design configuration. To configure that memory *.sof file is



used. SRAM is volatile memory, during every power cycle it is necessary to reprogram FPGA. FPGA can be configured automatically using external non volatile memory. These memories can be Compact Flash Memory cards or dedicated high density flash memory.

*.pof file is used to configure such non volatile memories. FPGA has capability to access these memories and its internal logic can configure SRAM from external memory. So no need to configure FPGA manually.

Step 1: Run Quartus Prime Lite

Step 2:

Go to "File Menu-> Convert Programming Files"



Page 182

Step 3:

In Convert Programming File window select

- a) Programming File Type as *.pof
- b) Configuration device (in my case EPCS64)
- c) Select path and file name for output file



| - there - Person | 1 | | | | Langt | allera sue |
|--|--|---|--|-----------------|--------------|---|
| u can also ingentis Nine also. Somensian setup 1 | ngut the information : Nes | from other Nex and save the car | verson sollt information of | eated twine for | | |
| | Open Conversion | Selap Dala | 20 | Bave Galves | sim Selah-+ | |
| Montprogramme | 9.94 | and a second second | | | | |
| logramming file by | pe: Cogienne (| Depict File Lag | | | | * |
| Ophine | Configuration | device: (TTCTRA) | | Note: | Active Serie | e •) |
| lenaries | Christen pol | > | | | | bed |
| Advancel | Interestation | update difference file. | NH. | | | · * |
| | | | | | | |
| | SE Create Me | many Map Pile Scienciale Months | nel | | | |
| | 2 Deale He | many Map Pile (Centrole Meson) If Rep Clemenole Inform periph a | nici of million one del | | | |
| put Res to come | R Greate Me | mary Hap File Schwale bitum. F Res Schwale bitum perph a | naci of and below-core staff | | | |
| put life) to conve Me | 2 Create Me | nere Map Rie Stevenste Maam. 7 Nei Stevenste biloon om phij Properties | naci uf and below over del Start Address | | | Add No. Date |
| put Ret to como File SOF Data | E Groate Me Desite Cr Dete arca | ner Hap File Serende blom File: Serende blom perph p Popertie: Fige.3 | ned af and bloan canol del Start Address Galda > | | | Add Han Date |
| pul Rei ti cona Pie SOF Data | R Create Me Create Cr of Data area | ners Hap Fle Screnzie Intern Flee Screnzie Internation Flee Screnzie Internation Properties Flags_3 | ned of and taken care dat Start Address Galation | | | Add Nex Date Add Sof Page July For |
| put Rei te conv File SCH Data | R Create Me Create Cr Dela Acta Data Acta | ner Har Ne Derende Hom. * De Derende skor orgen y Popertes Nar 3 | ned of and totals care dat Start Address cauda > | | | Add two Date |
| put file to como File SOF Data | St Oreate Me | ner Har Ne Derende Hom. 1 Bei Derende store orsen s Popertes Faier 3 | net ni mi tetan ore titt Start Address Gasta > | | 1 | Add two Date Add Sof Page Lot The Schure 10 |
| put Rei ti convi Ple SCF Data | St Deale No Deale Cr Prode Cr Refe atea | ner Martik Sinnak Maan Mar Sannak Man pryko Pogeta Nagrja | nect ni mit teken over kilt Start Address Gasta > | | | Add Has Date Add Sof Page Add Sof Page Add Tile Add Tile To Dear |
| put Rei to como rite SCP Data | St Deale No Deale Cr All Dela ana | mery May Net Schweste Mosen I Bei, Sonwork Inton preph Poger Se Poger 3 | ned of and bitan care diff Start Address Galace | | | Add Hao Date Add Sof Rep Add Sof Rep Remove 10 Deser Properties |
| npul Rei to como Pile 309 Dara | St Deale No Deale Cr At Data ana | ner Mertik Sanada krassa Naci Sanada kitari pripina Popertes Nagr 3 | ned of milliption core shift Start Address Galder | | | Add two Date Add out hape Add out hape Add the Reserve From the Reserve |

Step 4:

Now click on SOF Data as shown in below image and click on Add File

| | ig hile | | | | | 101 101 |
|--|----------------------------|---|--|------------------------|------------------|--|
| - Date - Neither | | | | | (any) | t altera com |
| si can also inport input fune solo. Conversion setup files | file information from pith | or Nee and sove the | carverson assus inhe | marken-created here fo | | |
| 1 0 | See Concesso Selas D | wa. | | Bave Carl | erstein Sellagin | |
| Output programming B | | | | | | |
| Programming file type: | Programmer Object Fil | k Loot | | | | * |
| Ophine | Configuration device: | B2284 | | • Note: | Active lies | e • |
| Ne varie: | C (bitain.pof | | | | | Ind |
| Advanced | Remote Auto update d | allerese lies | N.H. | | | · * |
| lead Bet burners | Constructed Res 02 | ererele information | h pol entitions com | and . | | |
| input Ret to convert | C) Create Cut Net 32 | enerois bilost perp | A of militize on | ant. | | Add New Date |
| Input Res to convert | Douecries | Properties | n gef milleton om Start A cantos | udet ma | 2 | Add tike Date |
| input Rei to convent Intellige Soli basis | | Popertes ar J | h pifeiltion on Satu Galas | olet Othera | | Add tites Detail Add Sof Page |
| Input Red to convert The Day SOF Data | Source of Reds | Properties (Properties (Properties) | n pri mi lotori con Statu Gada > | oldinas | | Add Has Date |
| inuit Rei to convert rise/basis | Douis Cirlies Si | Popertes Popertes 91,3 | n auf millioten een Start A Gadas | dð m | | And hiss Date |
| Intel Rei Is convert | | Properties Properties GP_3 | n auf milliotor-oor Start A Gada> | old m | | Add this Date Add Sof Page Add Sof Page Add Sof Page Add Take Add Sof Page Add Sof P |
| Input Res to convert | | Properties | n gof wellteton ove Stert A caelo> | off | | And this Units And Sof Page And The Barney The Deser |
| Input Res to convert | Double of Ne 20 | Properties Properties (P. 3 | A gal and block one Start A Galax | ed. | | And this Units And Sof Page And Frie Sector Tomat Properties |

Step 5:

Browse .sof file using Select Input File browser and click on Open





Step 6:

Now click on Generate button in Convert Programming File window

| Convert Programm | ing File | | | | | and the second |
|--|--|---|---|--------------------------|-----------------|---|
| le Tuoiz Window | | | | | 1.043 | not active for |
| ou can also inport inpu liture une. Commission setup files | it file information from | other Nex and save the co | everant with in | himation created here fo | S | |
| L | Open Conversion Set | kgi Della | | Bave Can | erstein Serlagt | |
| Ouburtangueners) | | | | | | |
| Programming file type | Programme Obse | ct like Lawn | | | | |
| Codure. | Configuration devi | or: (PC364 | | • Note: | Adveb | eid • |
| tie rate: | C./bitsin.pof | | | | | bei |
| I the second | T | a second second | N/NE | | | · 7 |
| averei | 10 Courts Manual | an alleverar te. Mar Die Verstein | | | | |
| Input Rei to convert | 2 Croate Hener Croate Coll No | e Map File Sienerste bitum o Sienerste bitum perph | angel gef måltelser so | ent | | |
| Input Res to convert Plesto | Research Local gala | e datement de. • Map Ne Serense biom • Generale biom proph Properties | smed ant mit tricks of Start | - off | | Add Nex Deter |
| accent | Armene (Lack upd St Oreate Mener Consta Coff Re rist area Minarh (2010/811a) | Page 3 Page 3 PAGE 101 | oragi pof millotori o Stati castar | e del | | Add Nos Deter |
| Input Res to convert Place • SCP Data DE2_115_51 | Sector Cardonador Sector Menore Construction Coll Re Na Artis Manah, 201208114 | Page 3 Provide Science How Develop How compt Page 3 (P421:127-25 | smet primitizano Stati Gadas | e fill Adhen | | Add Nos Dates Add Sol Page Juli File |
| Input Rick to convert Piedo • SOF Data DE2_115_50 | Remove (Lands upon SE Consile Mension Consile Coff Re Minarh, 2013/08/14. | Poperties Poperties Poperties Poperties Poperties | ungel per vel tetor vo Start cauto | e del | | Add Sof Page Add Sof Page Lott File Tempy |
| Input Ris to convert Pietos • scenaus DE2_115_50 | Armen Legende 2 Deste Kener Deste Cell In Annen 20100004 | Map Re Generate Mos Connect Monitoria Properties Page 3 B-4211973 | ungel per en lotter og Sørt caular | e del | | Add Not Date Add Sof Page Add Sof Page Reserve 10 |
| Input Res to convert Preds 4 SOFT (riss 052_(15_3) | Arrent Log (ed) | Page 5 Provide Michael Micae Connect Micae perph Page 5 Page 5 Pr4211973 | ungel per en lotter og Sært Gæder | e fill Adhen | | And this links And sof Page Link The Reserve 10 Theory |

Step 7: If everything is OK then QuartusII will show message of success





Step 8:

Programming .pof file to Serial Configuration Device

a) Connect FPGA board to PC using USB Cable (Make sure you have connected to USB Blaster)b) Select Serial Configuration Memory using slide switch(Prog Mode) on FPGA board and power on the FPGA board

c) Go to "Tools Menu->QuartusII Programmer" in QuartusII

d) Select "Mode" as "Active Serial Programming"

e) Click on Add file button and browse generated .pof file

f) Now Click on Start button. Programming may take couple of minutes. Time depends on size of the file

g) After successful operation power of the board and select "Run Mode" using slide switch instead of "Prog Mode". After powering on the board and you will find FPGA is working. Sometimes it happens that QuartusII Programmer fails to detect Byte Blaster (USB JTAG). In this case check whether drivers are installed on not. You may locate drivers in

"X:/altera/tool_version/quartus/drivers/usb-blaster-ii". X is the installation directory. In my case tool_version was 13.0.

Then Click on "Hardware Setup" button in QuartusII Programmer. In Available Hardware items you will find USB Blaster. Double click on USB Blaster and close the window. If you select USB Blaster properly the you will find name of USB Blaster next to the Hardware Setup Button in QuartusII Programmer.

Now you can program external configuration memory like EPCS64 using QuartusII Programmer with generated .pof file



