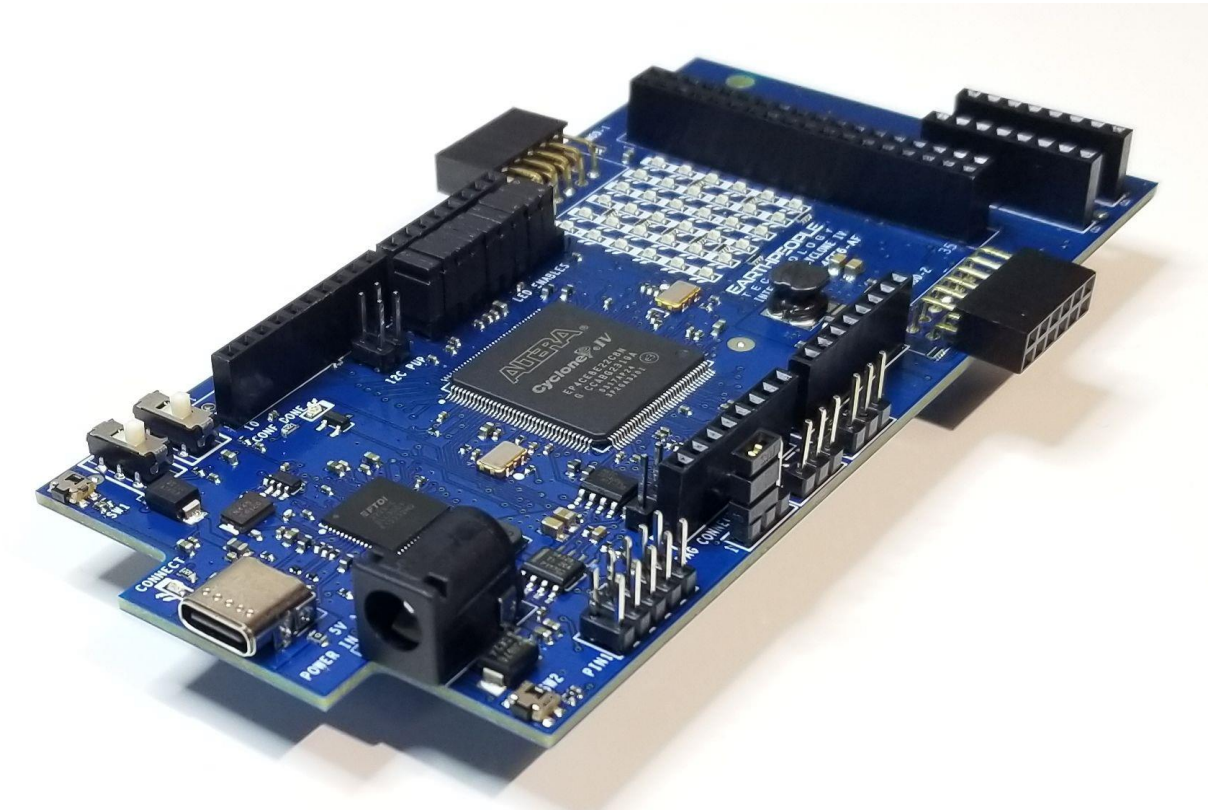
DUEPROLOGIC

FPGA DEVELOPMENT SYSTEM

Data Sheet



The DueProLogic (EPT-4CE6-AF-D2) is a part of the EPT USB/FPGA development system. It provides an innovative method of developing and debugging the users FPGA code. It can also

provide a high speed data transfer mechanism between microcontroller plug in board and Host PC.

The DueProLogic board is equipped with an Altera EP4CE6E22 FPGA; which is programmed using the Altera Quartus Prime software. The FPGA has 6,272 Logic Elements along with 276Kbits of RAM. An on board 66 MHz oscillator is used by the EPT-Active-Transfer-Library to provide data transfer rates of 8 Mega Bytes per second. The EPT-Active-Transfer-Library provides control communication between the objective device and the FPGA. Data transfer during the objective device checkout between the PC and the FPGA program is available via the ActiveHost. The board also includes the following parts.

- Altera EP4CE6 FPGA with 6272 Logic Cells
- Dual Channel High Speed USB FT2232H
- 66 MHz oscillator for driving USB data transfers and users code
- 100MHz oscillator for scaling up/down for users needs
- Standard SD Card interface for memory expansion
- 54 user Input/Outputs (+3.3V only)
- 36 Green LED Array accessible by the user
- Two PCB switches accessible by the user
- Two Slide switches
- Two PMOD Connectors

Block Diagram

Figure 1 EPT-4CE6-AF Component Location

Data Sheet EPT FPGA Development System

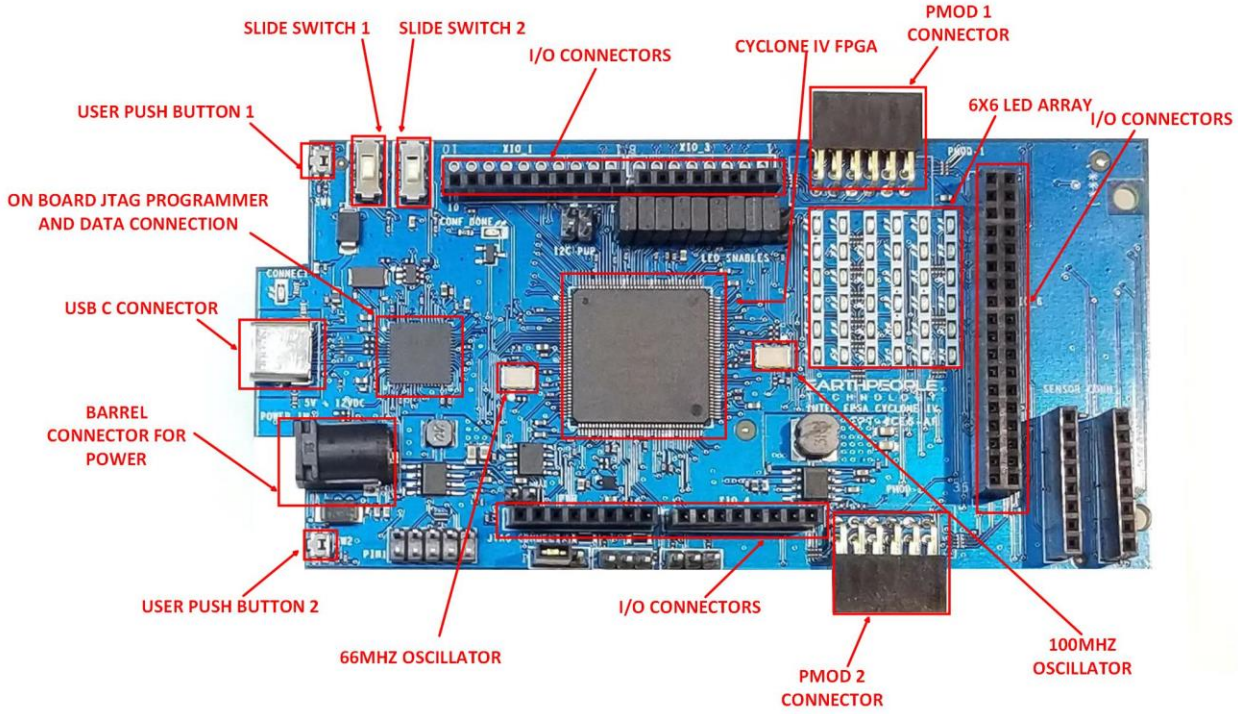
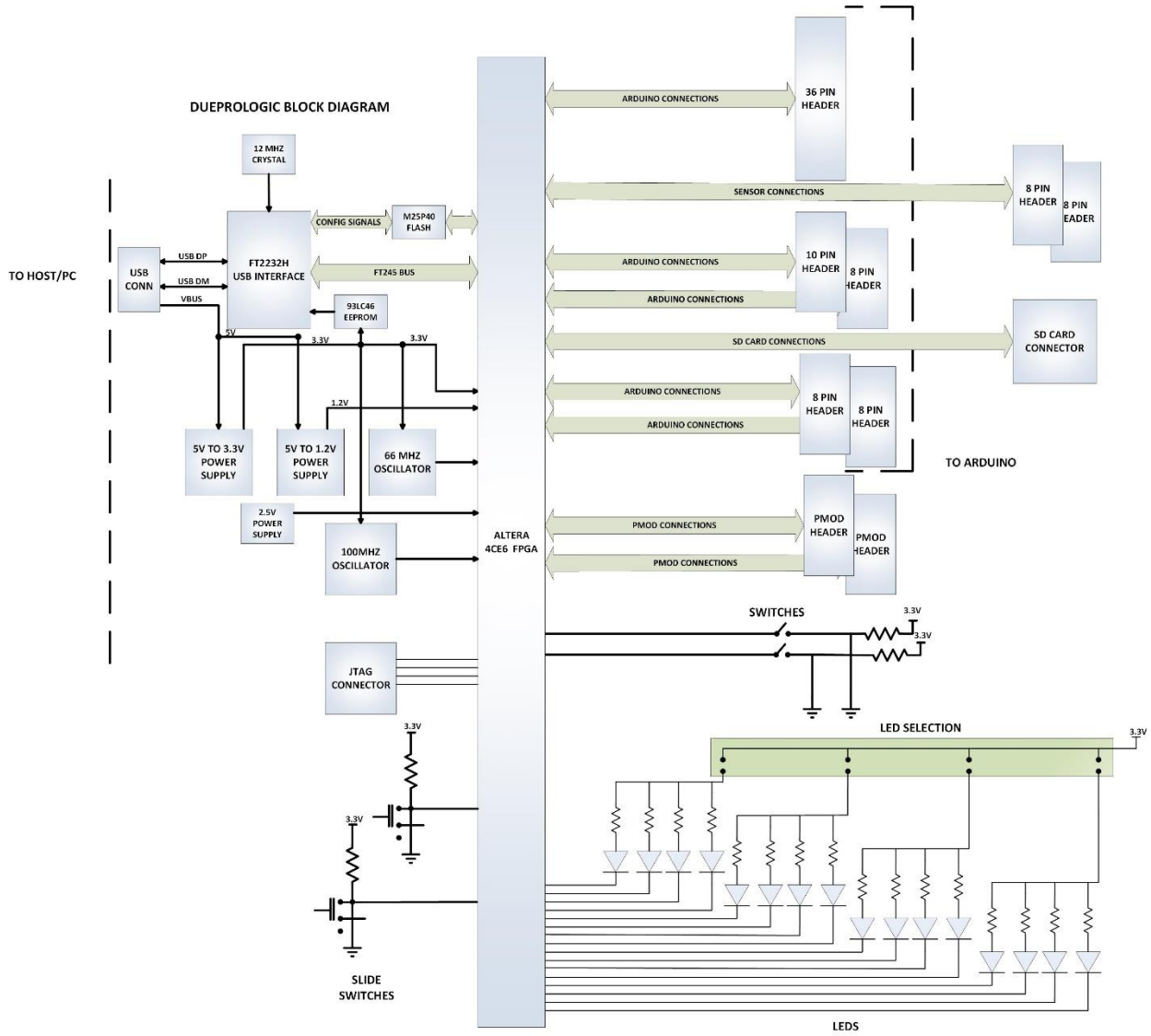


Figure 2 EPT-4CE6-AF Block Diagram

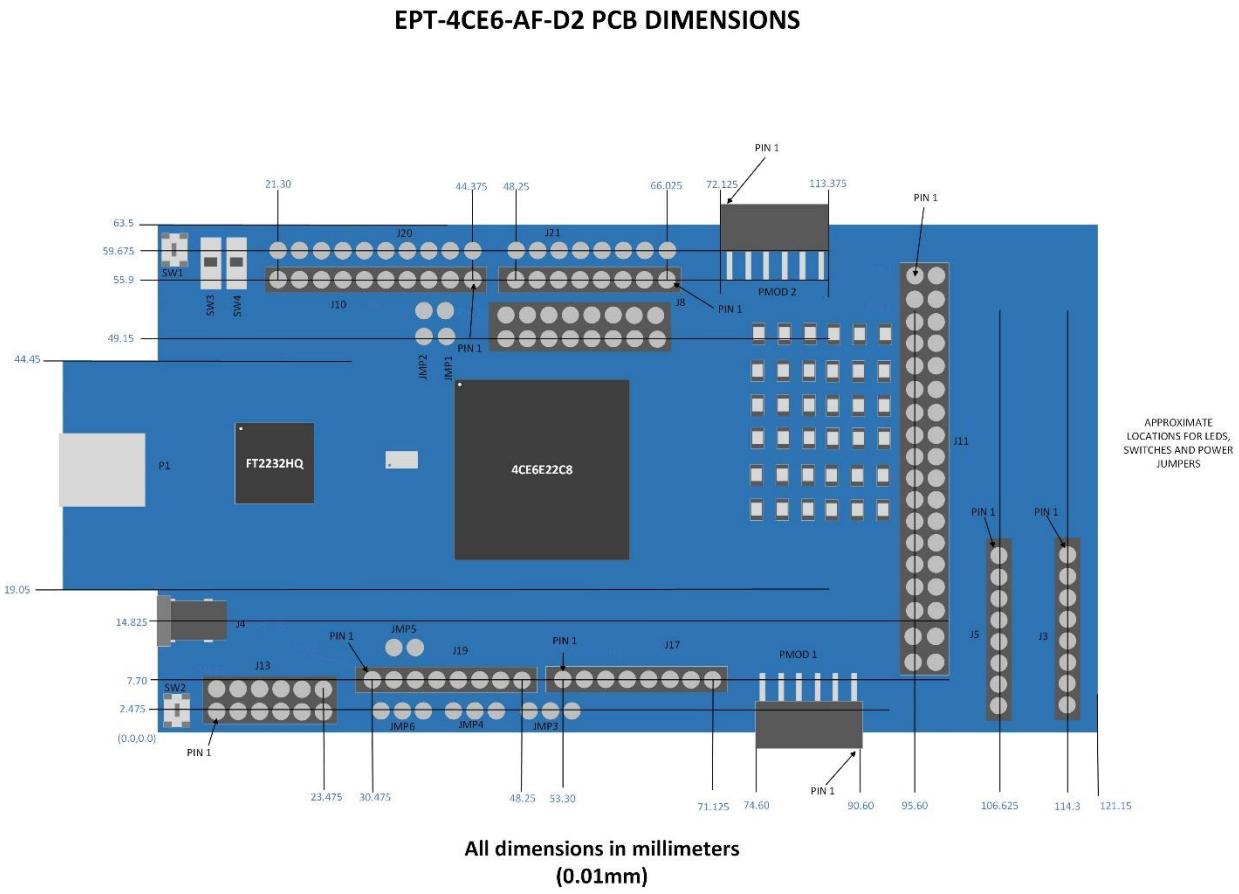


Data Sheet EPT FPGA Development System

The DueProLogic USB/FPGA Development System consists of an Altera FPGA, USB to Serial chip, Configuration flash, two separate oscillators, SD Card slot, two push buttons and 36 LEDs. The board has 63 User Input/Outputs available at 6 headers that match the Arduino Due board configuration. There are two power options, USB-C connector or Barrel Connector.

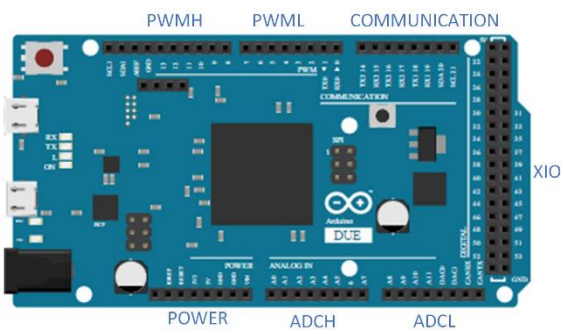
Mechanical Dimensions

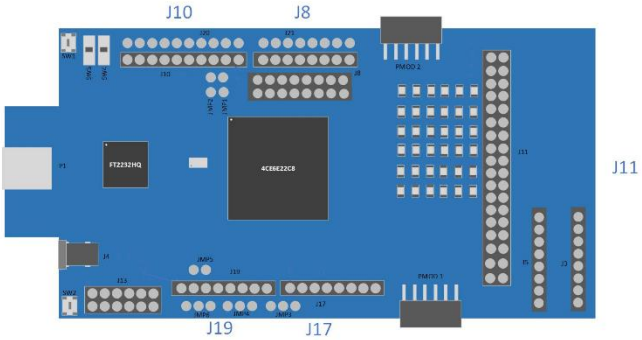
Figure 3 EPT-4CE6-AF Mechanical Dimensions



Pin Mapping

Figure 4. Pin Mapping between Arduino Due, DueProLogic and FPGA User code





Arduino Due Connector Pin	DuePrologic Connector-Pin #	DuePrologic Net Name	DuePrologic FPGA Pin Number	DuePrologic FPGA User Code Signal Name
D21	J10-1	UB0	136	XIO1[0]
D20	J10-2	UB1	137	XIO1[1]
AREF	J10-3	UB2	138	XIO1[2]
GND	J10-4	UB3	141	XIO1[3]
D13	J10-5	UB4	142	XIO1[4]
D12	J10-6	UB5	143	XIO1[5]
D11	J10-7	GND	NC	NC
D10	J10-8	3V3	NC	NC
D9	J10-9	UB6	144	XIO1 [6]
D8	J10-10	UB7	7	XIO1[7]

Arduino Due Connector Pin	DuePrologic Connector-Pin #	DuePrologic Net Name	DuePrologic FPGA Pin Number	DuePrologic FPGA User Code Signal Name
NC	PMOD_2-1	UB12	67	PMOD2[0]
NC	PMOD_2-2	UB11	66	PMOD2[1]
NC	PMOD_2-3	UB10	53	PMOD2[2]
NC	PMOD_2-4	UB9	52	PMOD2[3]
NC	PMOD_2-7	UB14	55	PMOD2[4]
NC	PMOD_2-8	UB13	54	PMOD2[5]
NC	PMOD_2-9	UB53	69	PMOD2[6]
NC	PMOD_2-10	UB52	70	PMOD2[7]

Arduino Due Connector Pin	DuePrologic Connector-Pin #	DuePrologic Net Name	DuePrologic FPGA Pin Number	DuePrologic FPGA User Code Signal Name
NC	PMOD_1-1	UB12	67	PMOD1[0]
NC	PMOD_1-2	UB11	66	PMOD1[1]

NC	PMOD_1-3	UB10	53	PMOD1[2]
NC	PMOD_1-4	UB9	52	PMOD1[3]
NC	PMOD_1-7	UB14	55	PMOD1[4]
NC	PMOD_1-8	UB13	54	PMOD1[5]
NC	PMOD_1-9	UB53	69	PMOD1[6]
NC	PMOD_1-10	UB52	70	PMOD1[7]
Arduino Due Connector Pin	**DuePrologic Connector-Pin #**	**DuePrologic Net Name**	**DuePrologic FPGA Pin Number**	**DuePrologic FPGA User Code Signal Name**
D7	J8-1	3V3	NC	NC
D6	J8-2	UB16	127	XIO3[0]
D5	J8-3	UB17	128	XIO3[1]
D4	J8-4	UB18	129	XIO3[2]
D3	J8-5	UB19	132	XIO3[3]
D2	J8-6	UB20	133	XIO3[4]
D1	J8-7	UB21	135	XIO3[5]
D0	J8-8	GND	NC	NC

Arduino Due Connector Pin	DuePrologic Connector-Pin #	DuePrologic Net Name	DuePrologic FPGA Pin Number	DuePrologic FPGA User Code Signal Name
D54	J17-1	VIN	NC	NC
D55	J17-2	UB65	31	XIO4[0]
D56	J17-3	UB64	46	XIO4[1]
D57	J17-4	UB63	44	XIO4[2]
D58	J17-5	UB62	42	XIO4[3]
D59	J17-6	UB61	49	XIO4[4]
D60	J17-7	UB60	50	XIO4[5]
D61	J17-8	GND	NC	NC

Arduino Due Connector Pin	DuePrologic Connector-Pin #	DuePrologic Net Name	DuePrologic FPGA Pin Number	DuePrologic FPGA User Code Signal Name
NC	J3-1	3V3	NC	NC
NC	J3-2	UB54	119	XIO5[0]
NC	J3-3	UB55	120	XIO5[1]
NC	J3-4	UB56	121	XIO5[2]
NC	J3-5	UB57	124	XIO5[3]

NC	J3-6	UB58	125	XIO5[4]
NC	J3-7	UB59	126	XIO5[5]
NC	J3-8	GND	NC	NC

Arduino Due Connector Pin	**DuePrologic Connector-Pin #**	**DuePrologic Net Name**	**DuePrologic FPGA Pin Number**	**DuePrologic FPGA User Code Signal Name**
	J11-1	3V3	NC	NC
	J11-2	VIN	NC	NC
	J11-3	UB22	115	XIO6[0]
	J11-4	UB23	114	XIO6[1]
	J11-5	UB24	113	XIO6[2]

	J11-6	UB25	112	XIO6[3]
	J11-7	UB26	111	XIO6[4]
	J11-8	UB27	110	XIO6[5]
	J11-9	UB28	106	XIO6[6]
	J11-10	UB29	105	XIO6[7]
	J11-11	UB23	104	XIO6[8]
	J11-12	UB31	103	XIO6[9]
	J11-13	UB32	101	XIO6[10]
	J11-14	UB33	100	XIO6[11]
	J11-15	UB34	99	XIO6[12]
	J11-16	UB35	98	XIO6[13]
	J11-17	UB36	58	XIO6[14]
	J11-18	UB37	51	XIO6[15]
	J11-19	UB38	65	XIO6[16]
	J11-20	UB39	87	XIO6[17]
	J11-21	UB40	86	XIO6[18]
	J11-22	UB41	85	XIO6[19]
	J11-23	UB42	84	XIO6[20]
	J11-24	UB43	83	XIO6[21]

	J11-25	UB44	80	XIO6[22]
	J11-26	UB45	77	XIO6[23]
	J11-27	UB46	76	XIO6[24]
	J11-28	UB47	73	XIO6[25]
	J11-29	UB48	74	XIO6[26]
	J11-30	UB49	75	XIO6[27]
	J11-31	UB50	72	XIO6[28]
	J11-32	UB51	71	XIO6[29]
	J11-33	UB52	70	XIO6[30]
	J11-34	UB53	69	XIO6[31]

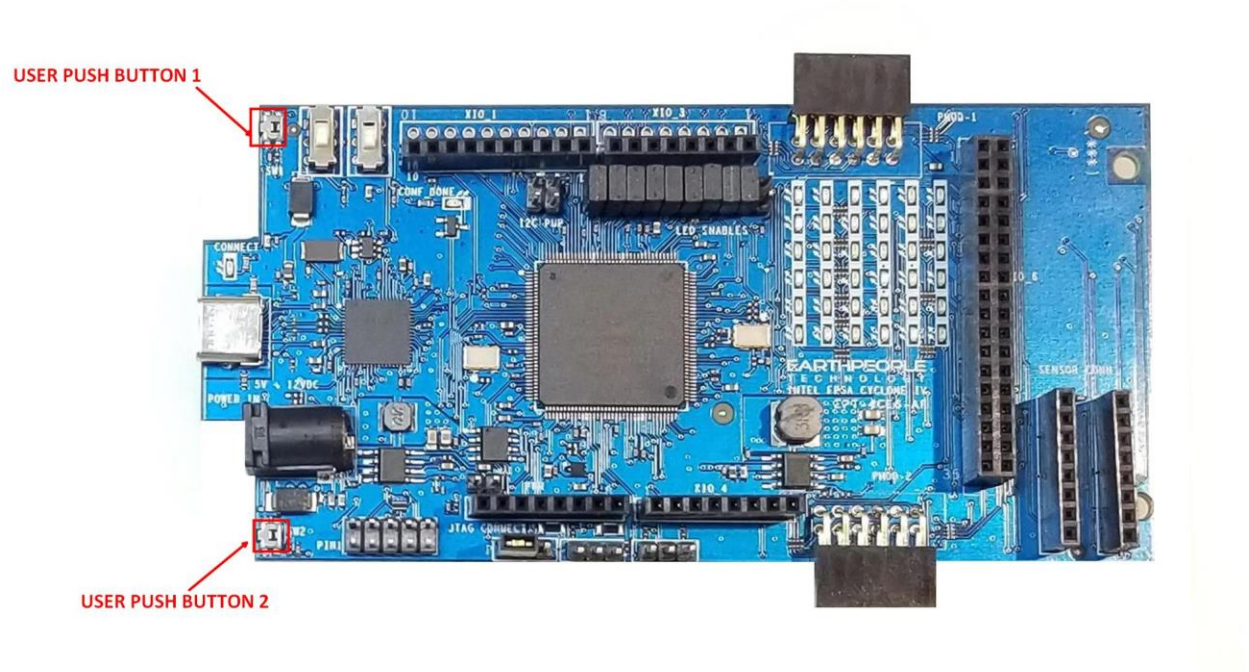
Arduino Due Connector Pin	**DuePrologic Connector-Pin #**	**DuePrologic Net Name**	**DuePrologic FPGA Pin Number**	**DuePrologic FPGA User Code Signal Name**
NC	J5-1	3V3	NC	NC
NC	J5-2	UB52	70	NC
NC	J5-3	UB50	72	NC
NC	J5-4	UB48	74	NC
NC	J5-5	UB71	59	XIO7[3]
NC	J5-6	UB70	60	XIO7[2]

NC	J5-7	UB55	120	
NC	J5-8	GND	NC	

Pushbutton switches

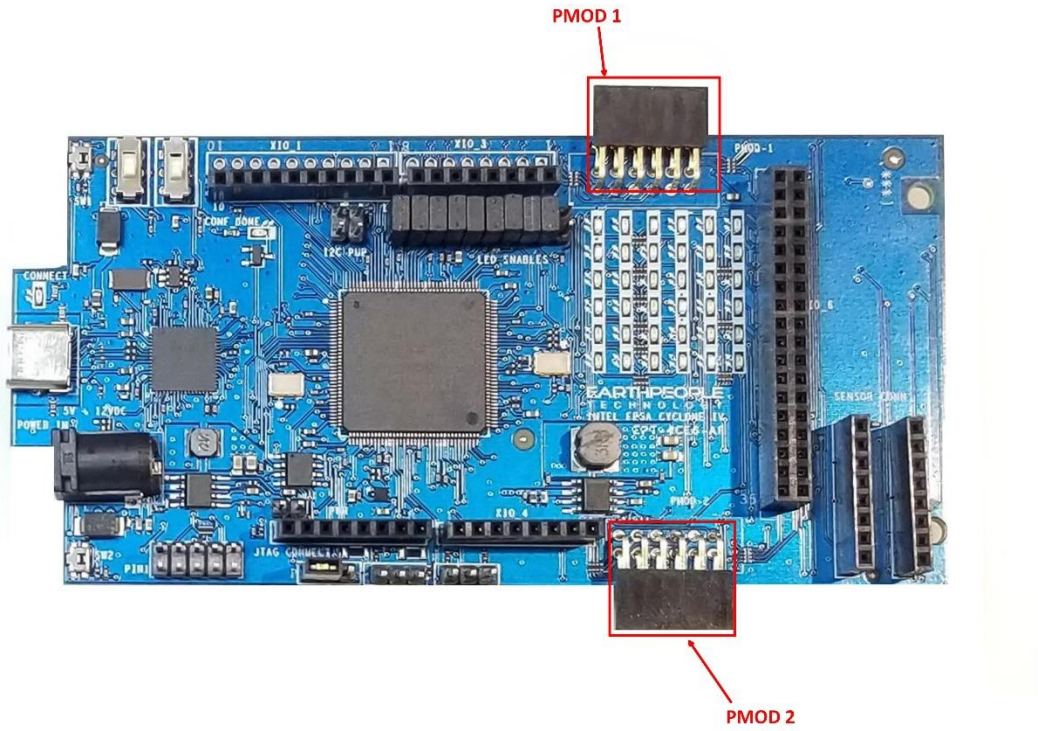
There are two pushbutton switches on the DueProLogic. Both are momentary contact switches. They include a 1uF cap to ground to debounce both switches.

Component	**Net Name**	**Pin on FPGA**	**Signal in EPT Project Pinout**	
SW1	UB66	25	UBA	
SW2	UB67	24	UBB	

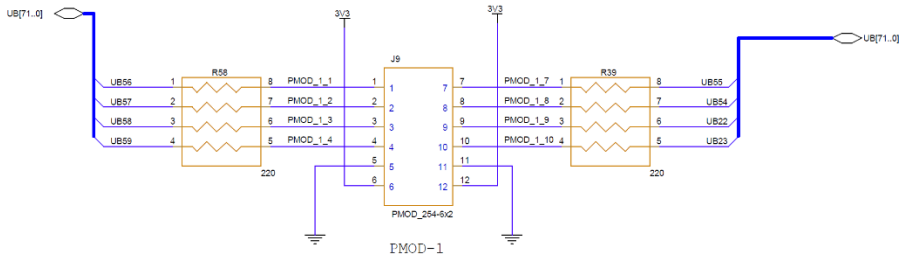


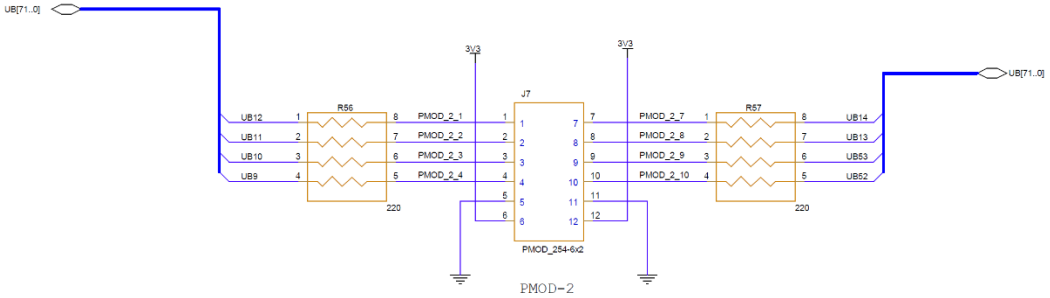
PMOD Connectors

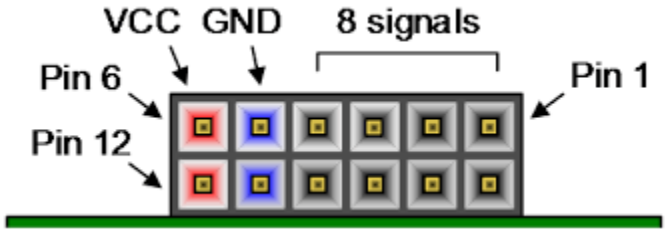
The DueProLogic includes two PMOD Connectors. These two connectors are located towards the rear of the board.



The PMOD pinouts follows the standard pinout. Pin 1 is located in the upper right when facing the connector.







VCC is +3.3V and the Inputs and Outputs of the 8 signals are +3.3V only. The eight I/O's are connected directly to FPGA pins and can be designated as any communications standard.

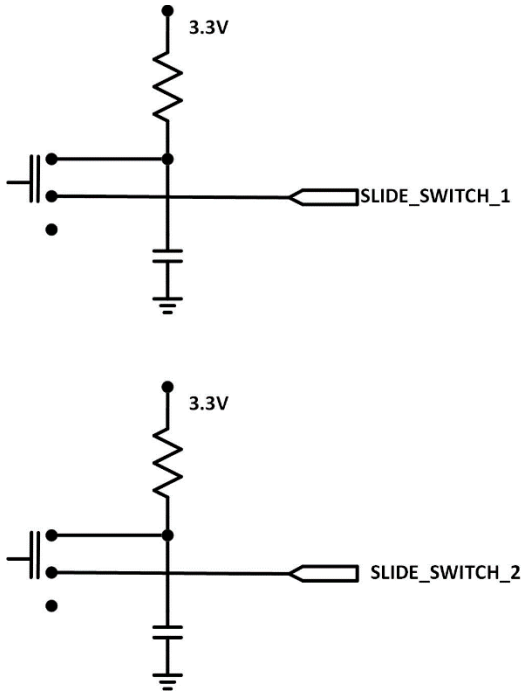
The PMOD have the following connections to the Cyclone IV chip:

PMOD Pin Number	Signal Name	Cyclone IV Pin Number
1-1	UB56	121
1-2	UB57	124
1-3	UB58	125
1-4	UB59	126
1-7	UB55	120
1-8	UB54	119
1-9	UB22	115
1-10	UB23	114
2-1	UB12	67
2-2	UB11	66
2-3	UB10	53
2-4	UB9	52
2-7	UB14	55
2-8	UB13	54
2-9	UB53	69

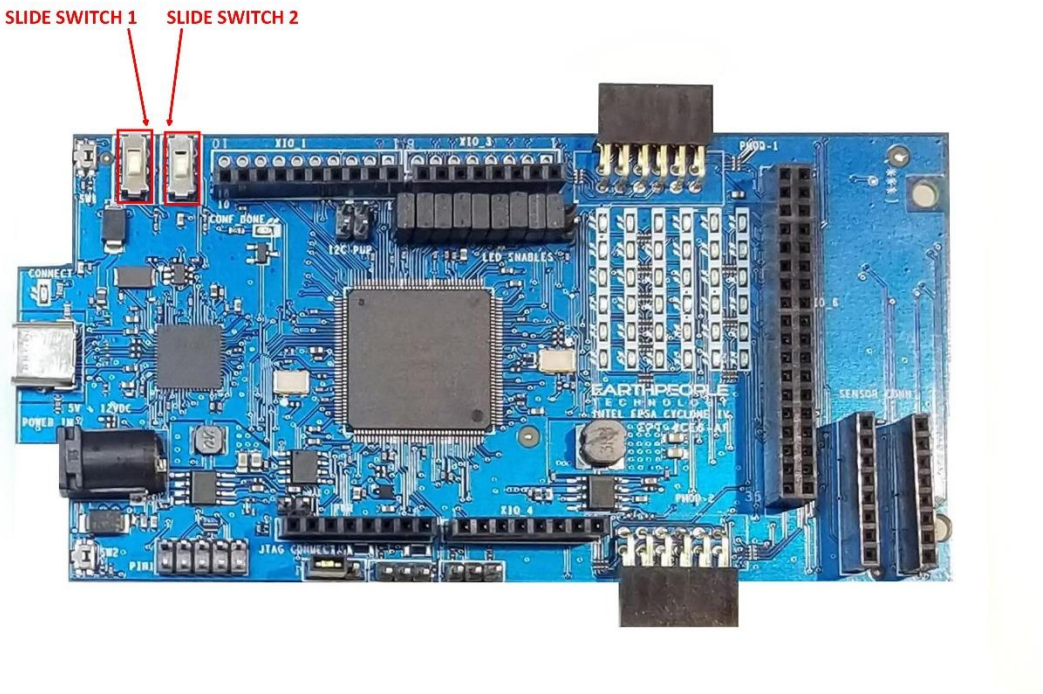
2-10	UB52	70

Slide Switches

The DueProLogic includes two slide switches. Both are full contact switches. They include a 1uF cap to ground to debounce both switches.



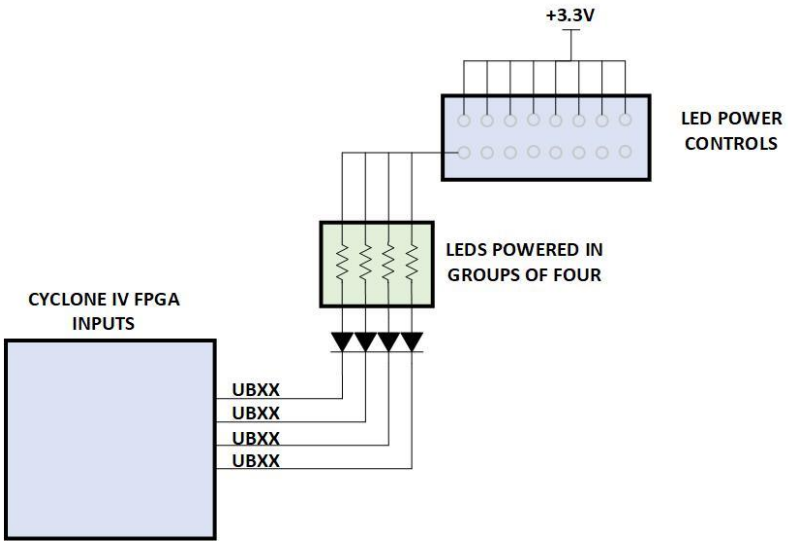
The slide switches provide a connection to either +3.3V in position 1or Ground in position 2.



Component	Net Name	Pin on Cyclone IV
SW3	SLIDE_SWITCH_1	91
SW4	SLIDE_SWITCH_2	90

LEDs

There are 38 total LEDs on the DueProLogic. One Green LED to denote when the Windows PC has discovered and enumerated the DueProLogic. One Green LED to denote when the Cyclone IV FPGA has been configured properly. And 36 Green LEDs for user programming. The 36 Green User LEDs are sinked directly from the Cyclone IV FPGA. Each LED uses a 220 Ohm resistor connected to +3.3V. The LED is driven with 5.4 mA's of current. There is also a jumper selectable power enable for each four block group of LEDs. This allows the user to turn off the LEDs and use the FPGA pin as Input/Output on the 36 pin connector.

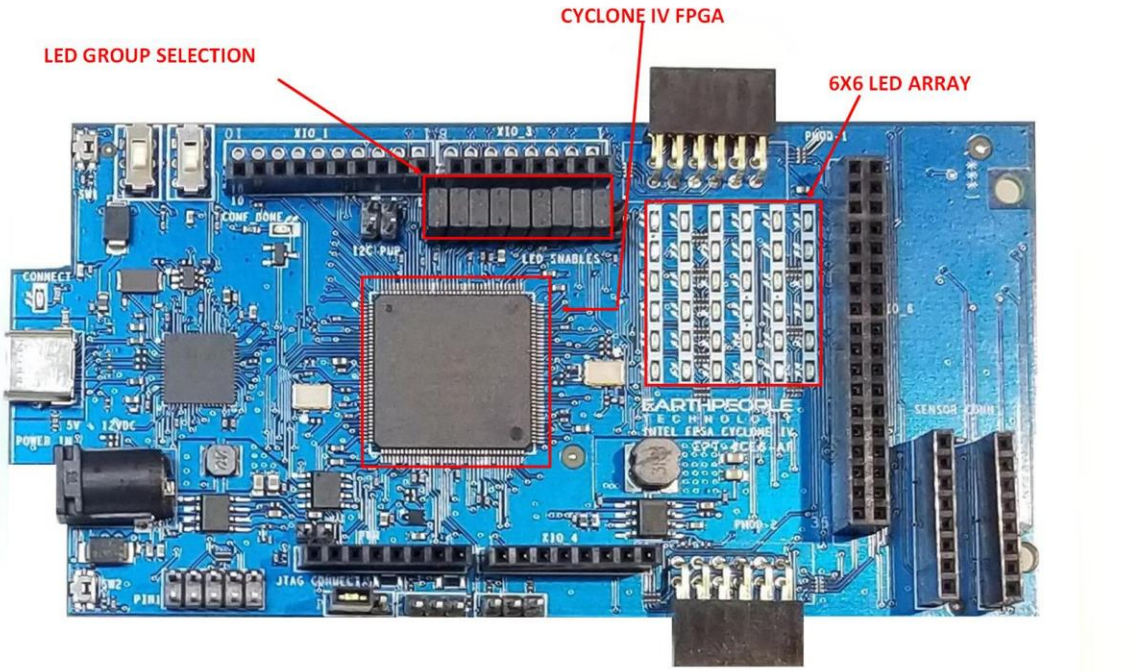


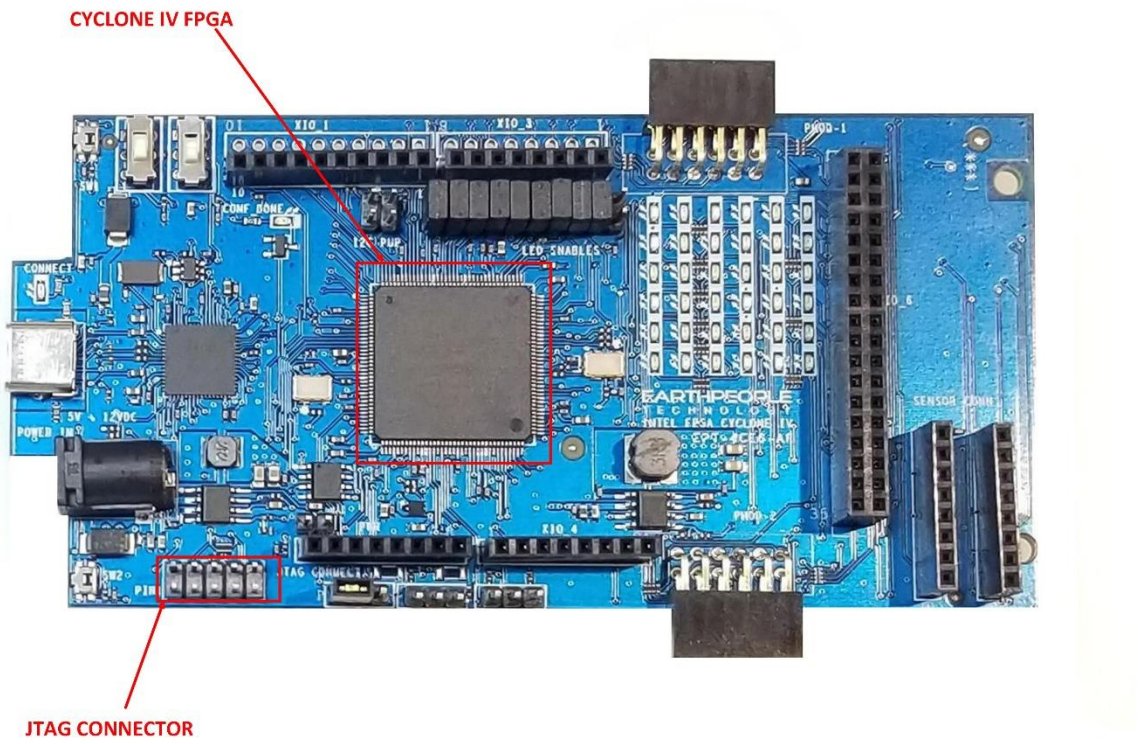
Component	Net Name	Pin on FPGA	Signal in EPT Project Pinout
LED0	UB22	115	XIO_6 [0]
LED1	UB23	114	XIO_6 [1]
LED2	UB24	113	XIO_6 [2]

LED3	UB25	112	XIO_6 [3]
LED4	UB26	111	XIO_6[4]
LED5	UB27	110	XIO_6[5]
LED6	UB28	106	XIO_6[6]
LED7	UB29	105	XIO_6[7]
LED8	UB30	104	XIO_6 [8]
LED9	UB31	103	XIO_6 [9]
LED10	UB32	101	XIO_6 [10]
LED11	UB33	100	XIO_6 [11]
LED12	UB34	99	XIO_6[12]
LED13	UB35	98	XIO_6[13]
LED14	UB36	58	XIO_6[14]
LED15	UB37	51	XIO_6[15]
LED16	UB38	65	XIO_6 [16]
LED17	UB39	87	XIO_6 [17]
LED18	UB40	86	XIO_6 [18]
LED19	UB41	85	XIO_6 [19]
LED20	UB42	84	XIO_6[20]
LED21	UB43	83	XIO_6[21]

LED22	UB44	TBD	XIO_6[22]
LED23	UB45	77	XIO_6[23]
LED24	UB46	76	XIO_6 [24]
LED25	UB47	73	XIO_6 [25]
LED26	UB48	74	XIO_6 [26]
LED27	UB49	75	XIO_6 [27]
LED28	UB50	72	XIO_6[28]
LED29	UB51	71	XIO_6[29]
LED30	UB52	70	XIO_6[30]
LED31	UB53	69	XIO_6[31]
LED32	UB68	68	XIO_7[0]
LED33	UB69	64	XIO_7[1]
LED34	UB70	60	XIO_7[2]
LED35	UB71	59	XIO_7[3]

Data Sheet EPT FPGA Development System

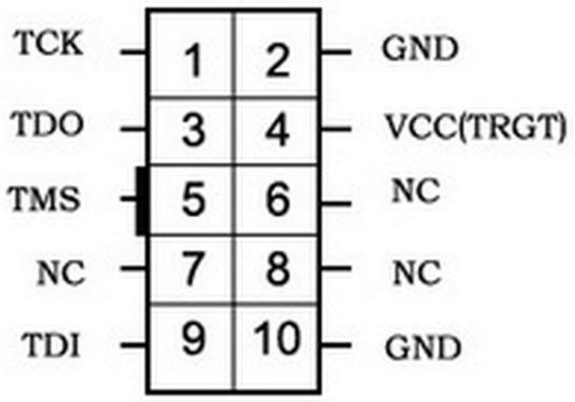




JTAG Header

A 10 pin, 5x2 connector is included on the DPL to provide JTAG programming of the Cyclone IV. The default programming method is via the Configuration Flash. JTAG programming the FPGA directly is provided as a secondary option. An external programmer must be used access this JTAG header. The header follows the standard Intel FPGA pinout. So, any USB Blaster compatible programmer can be used to connect directly to this header and program the FPGA. No other jumpers or configuration is needed, just connect the programmer and the Quartus software will recognize the FPGA.

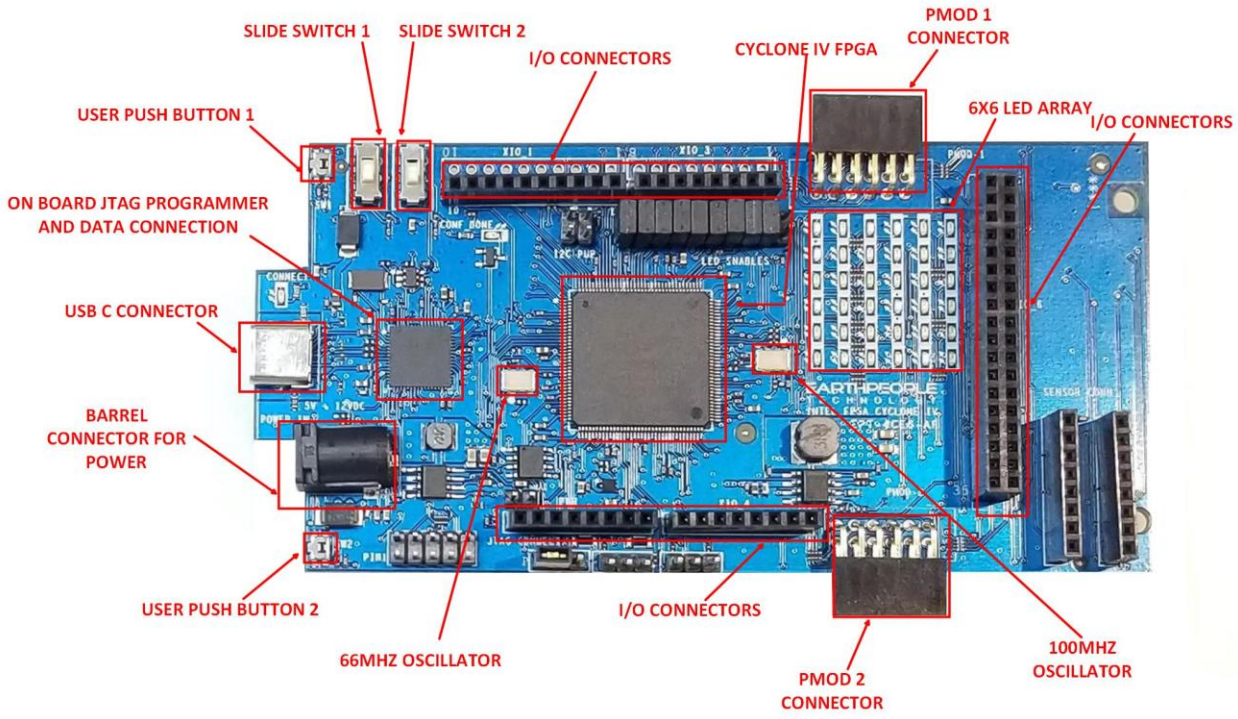
JTAG connector pinout:



Cyclone IV FPGA

The DueProLogic includes the Intel FPGA EP4CE6E22C8N, operating internally with 1.2V and 2.5V, and externally at 3.3V being 3.3V tolerant. Operates corner to corner logic in 9ns. 392 configurable logical/logic array blocks, 6272 logical elements/cells, 270Kbit internal RAM, 15 multipliers to support DSP processing-intensive applications, 2 PLLs.

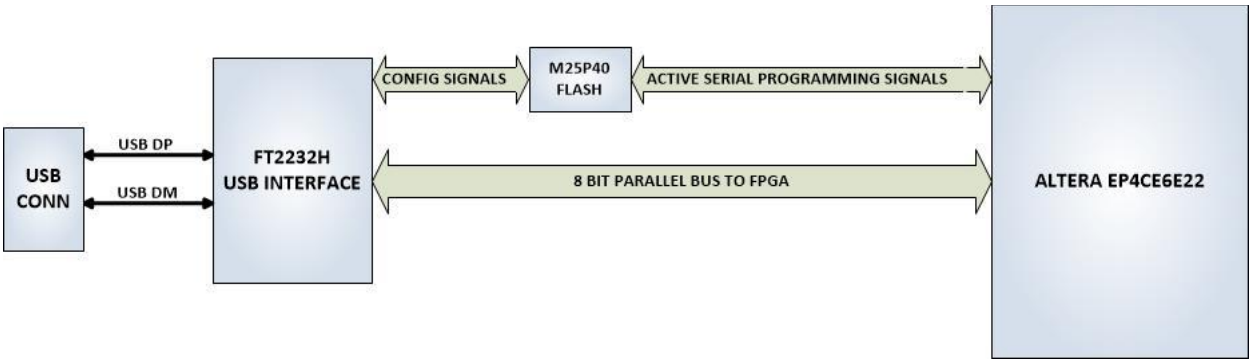
Inputs/Outputs



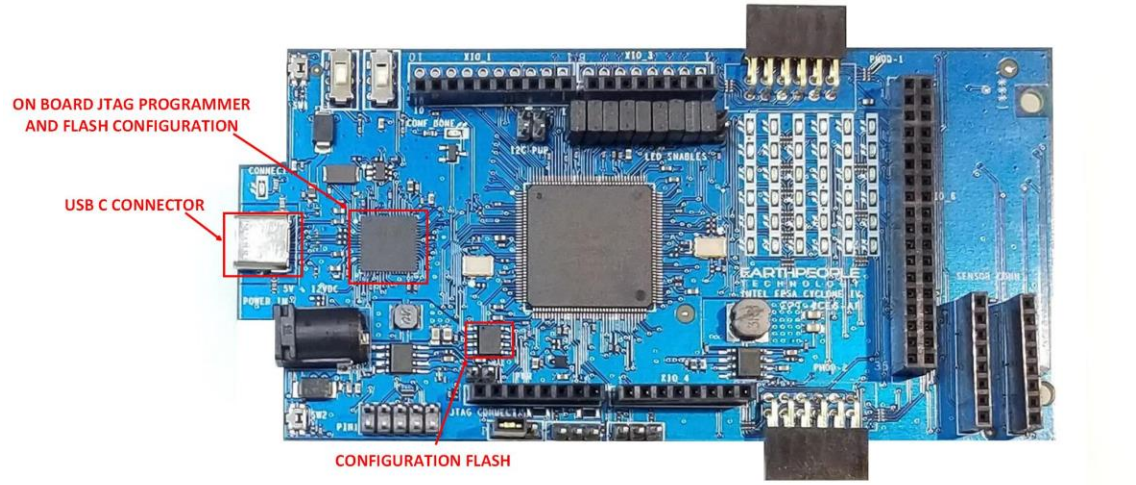
All I/O's are +3.3V only. Do not apply any voltage greater than +3.3V to the FPGA I/O's. All of the FPGA I/O's have been brought out to 0.1 inch socket/headers. These headers easily allow jumper wire to connect from connector to the FPGA pins. Selected headers also have a power pin and a ground pin. This allows the user to assemble a small connector with both power and signals to connect to external sensor boards.

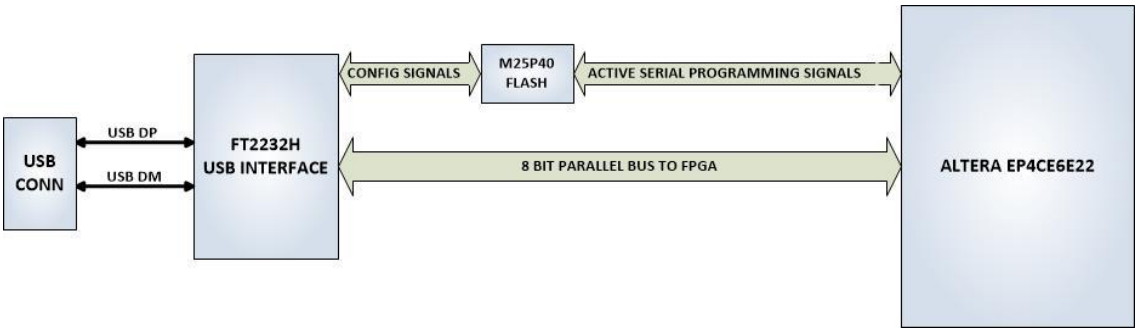
FPGA Configuration

The EPT Blaster Driver will allow the Quartus Prime Software to program the Configuration Flash chip on the DueProLogic. The software will only access the M25P40 Flash chip. This chip is accessed from the FT2232H USB chip. Quartus will store the compiled and synthesized user code. After programming is complete, the FPGA automatically resets and reads the code from the Flash chip and programs itself using the Active Serial method.



The Cyclone IV FPGA is configured for operation when the power is applied to the board. A dedicated Configuration Flash chip is included on the DueProLogic for the purpose of configuring the FPGA on power up. The DPL uses the second channel of the FT2232H chip as a dedicated Flash programming port. The Configuration Flash can be





programmed directly from Quartus Prime by using the EPT-Blaster driver. Follow the instructions in the “EPT Drivers” section of this manual. Follow the instructions in the section “Setting up the Project and Compiling” to program the flash on the DPL.

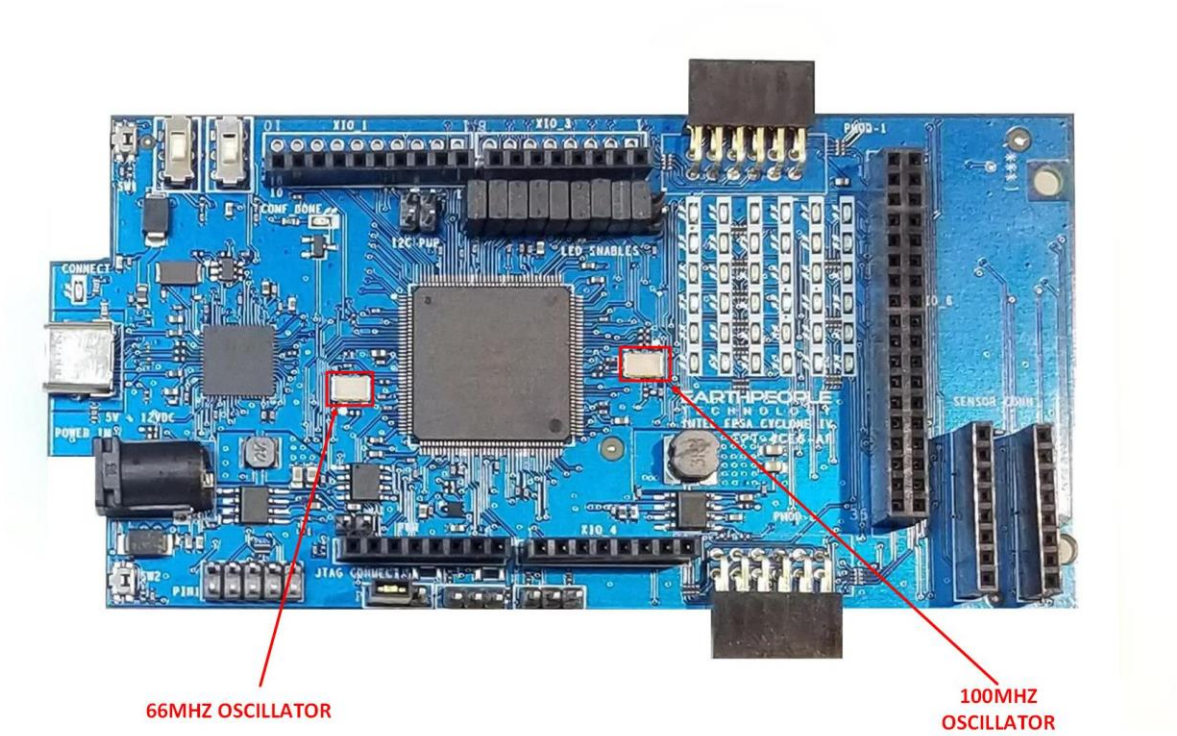
Oscillators

There are two oscillators on the DueProLogic, 66MHz and 100MHz. These oscillators have the following Vendor and P/N

1. 66MHz, Renesas Electronics America Inc; P/N: XLH536066.000000I
2. 100MHz, Renesas Electronics America Inc; P/N: XLH536100.000000I

These oscillators are connected to the Global Clock inputs on the FPGA. Both devices provide stable clock for the FPGA's internal DLL's. The user can access these clock sources by calling the net connected to the FPGA pin.

Component	Net Name	Pin on FPGA	Signal in EPT Project Pinout	
66MHz Osc	GCLK1	23	aa[1]	
100MHz Osc	GCLK7	88	CLK_100	



XLH536066.000000I

PARAMETERS	MAX (unless otherwise noted)
Frequency	66MHz
Supply Voltage (VDD)	3.3V
Input Current (IDD) >50.000 ~ 67.000MHz	 25 mA
Standby Current	10 µA
Output Symmetry (50% VDD) >50.000 ~ 170.000MHz	 40% ~ 60%
Rise/Fall Time (10%/90% VDD Levels) (TR/TF) 1.000 ~ 80.000MHz	 6 nS
Output Voltage (VOL) (VOH)	10% VDD 90% VDD Min
Output Load (HCMOS)	15 pF
Start-up Time (TS)	10 mS
Frequency Stability	±25ppm
Operating Temperature	-40°C ~ 85°C

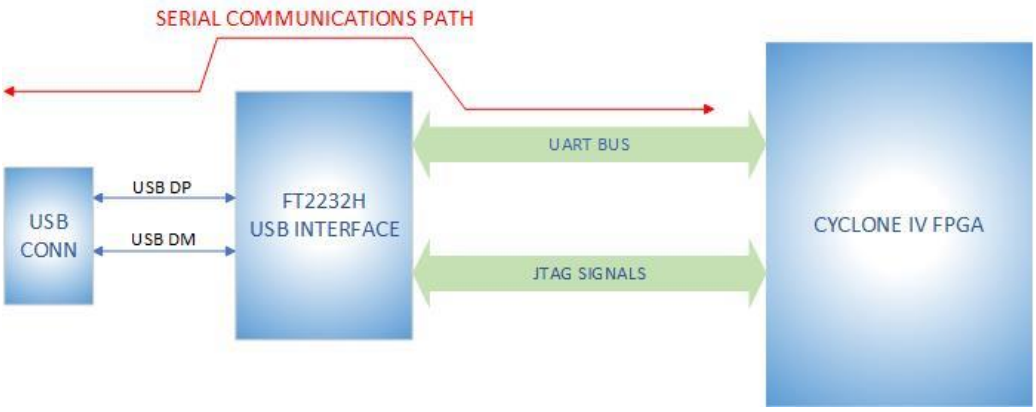
XLH536100.000000I

PARAMETERS	MAX (unless otherwise noted)
Frequency	100MHz
Supply Voltage (VDD)	3.3V
Input Current (IDD) >50.000 ~ 67.000MHz	47 mA
Standby Current	10 µA
Output Symmetry (50% VDD) >50.000 ~ 170.000MHz	40% ~ 60%
Rise/Fall Time (10%/90% VDD Levels) (TR/TF) 1.000 ~ 80.000MHz	6 nS
Output Voltage (VOL) (VOH)	10% VDD 90% VDD Min
Output Load (HCMOS)	15 pF
Start-up Time (TS)	10 mS
Frequency Stability	±25ppm
Operating Temperature	-40°C ~ 85°C

USB to Serial

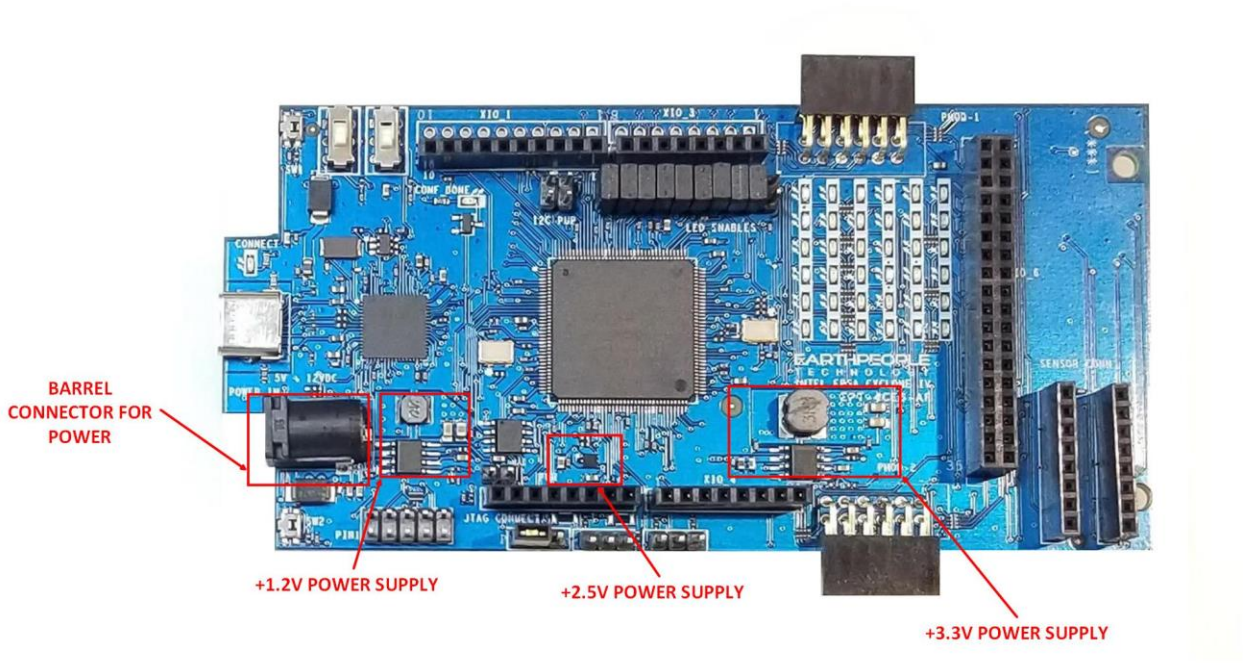
The FT2232HQ is a USB 2.0 High Speed (480Mb/s) to UART/MPSSE IC. The device features two interfaces that can be configured for asynchronous or synchronous serial or parallel FIFO interfaces. The two channels can also be independently configured to use an MPSSE engine. This allows the two ports of the FT2232HQ to operate independently as UART/Bit-Bang ports or MPSSE engines used to emulate JTAG, SPI, I2C, Bit-bang or other synchronous serial modes.

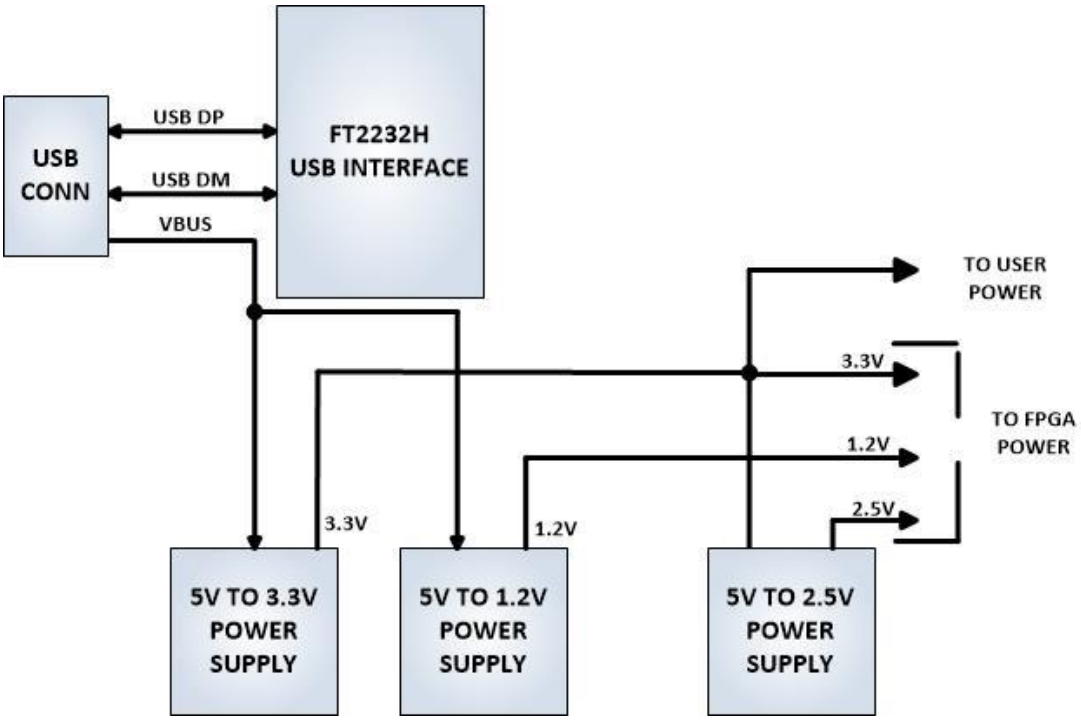
The chip is powered by +3.3V and includes an internal +1.8V regulator to power the chip core. It uses +3.3V I/O interfacing and is+5V Tolerant. Operational configuration mode and USB Description strings configurable in external EEPROM over the USB interface. USB to parallel FIFO transfer data rate up to 8 Mbyte/Sec. FT245B-style FIFO interface option with bi-directional data bus and simple 4 wire handshake interface. Asynchronous serial UART interface option with full hardware handshaking and modem interface signals. Fully assisted hardware or X-On / X-Off software handshaking. UART Interface supports 7/8 bit data, 1/2 stop bits, and Odd/Even/Mark/Space/No Parity.



DueProLogic Power

The DueProLogic can be powered from the USB bus of a Host/PC or the optional barrel connector. The USB supplies a maximum of +5V @ 500mA's. The components of the DueProLogic must share this power with the user code that will run inside the FPGA along with any external power use.


BARREL CONNECTOR FOR POWER
+1.2V POWER SUPPLY
+2.5V POWER SUPPLY
+3.3V POWER SUPPLY



Core Board Power Budget

Device	**Part Number**	**+1.2V Power**	**+2.5V Power**	**+3.3V Power**
FPGA	EP4CE6E22	??? Defined by user code. EPT-Transfer-Demo code: 50mA	10mA	??? Defined by user code. . EPT-Transfer-Demo code: 50mA
Flash	M25P40			15mA (During the Write

				Status, Sector Erase, and Bulk Erase cycles)
USB Chip	FT2232H			60 mA (no sink current supplied to I/O's)
USB EEPROM	93LC56			2 mA (write current) 1 mA (read current)
66MHz Oscillator	FXO-HC536R-66			47 mA
100MHz Oscillator	FXO-HC536R-100			47 mA
User LEDs				216 mA
CONF_DONE Green LED				5 mA
CONNECT Green LED				5mA
Total		**50mA**	**10mA**	**261mA**

*Theoritical Values only. This data needs to be validated

Core Board VUSB Power Budget

Device	**Part Number**	**VUSB**		
+1.2V Power Supply	TPS54229	70mA		
+2.5V Power Supply	AP7331	12mA		
+3.3V Power Supply	TPS54229	275mA		
Total		**357mA**		

* Theoritical Values only. This data needs to be validated