

# EARTH PEOPLE TECHNOLOGY, Inc

# BEEPROLOGIC DEVELOPMENT SYSTEM User Manual

The BeeProLogic is a CPLD development board that is designed to be user friendly and a great introduction into digital design for Electrical Engineering students and hobbyists. This board provides a simplified method for debugging programmable logic code. It has been designed with plenty of LEDs and Pushbuttons to allow a large amount of interaction between user and hardware operations. The board provides a convenient, user-friendly work flow by connecting seamlessly with Intel's Quartus Prime software. The user will develop the code in the Quartus environment on a Windows Personal Computer. The programmable logic code is loaded into the CPLD using only the Quartus Programmer tool.

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# **1** Introduction

The Earth People Technology BeeProLogic CPLD development system hardware consists of a a CPLD, 8Mb Flash and a single channel DAC. The board requires an external JTAG Programmer compatible with the JTAG Blaster. The Core of the board is the MAX V chip. The board can be powered by standard USB Micro B connector. There is a 10MHz oscillator attached to the MAX V chip for clocking user code. The board also includes 10 Green User LEDS, Seven User Pushbuttons and One external connector with six pins for GPIO.

# 2 User Setup

The BeeProLogic is ready to go straight out of the box. Just connect power from a PC/Laptop. Next, connect a JTAG Blaster or an Intel USB Blaster to J7 for programming the MAX V chip. Please note, the BeeProLogic comes with an adapter to convert the six pin JST connector at J7 to the ten pin 0.1 Inch 5x2 header with the JTAG Blaster standard pinout. Then, write some code, synthesize, and program the chip. See section x for details about programming the BeeProLogic board.



# **3** BeeProLogic Description

3.1 Functional Block Diagram



# 3.2 BeeProLogic Specifications

- MAX V 5M240ZT100 CPLD From Intel/ 240 Logic Elements;
- 8 Mbit Flash Chip
- 8 bit Single Channel DAC
- 5 Inputs/Outputs available at 8x1 connector on board
- 11 Green User configurable LEDs
- 8 User Configurable Pushbutton Switch
- Power: Standard USB (+5V @ 2Amp) Using Micro-B connector
- 10MHz Oscillator
- Standard Programming Connector fits any JTAG Blaster





# 3.3 CPLD

The BeeProLogic includes the Intel 5M240ZT100 CPLD. It is an PQFP 100 pin package. This CPLD incorporates 240 Logic Cells in the chip. The chip is programmed via JTAG and is compatible with the standard JTAG Blaster. Connector J7 on the rear of the board is the JTAG Connector. It is a JST 6x1 connector and the BeeProLogic includes an adapter to convert the 6x1 pins into the standard 5x2 JTAG Blaster connector.

# 3.4 Power Supply

The BeeProLogic is designed to be operated from the following power source:

• Standard USB Micro-B cable

The board has a Molex style USB Micro-B connector on board. Connect the USB cable either to a USB Port on a PC or a standard charger (+5V @ 2A). This provides power for two high-efficiency serial regulators (LDO) on-board. A +3.3V LDO provides power for the CPLD and other devices on the board. The +1.8V LDO provides power for the core of the CPLD.











## 3.5 Clock Domains

There is one clock domain external to the MAX V CPLD, 10 MHz. The 10 MHz oscillator is a +3.3VDC device that provides a high speed clock to the CPLD. It is a CMOS device that provides a stable 10 MHz at  $\pm 50$  ppm. This clock can be used directly in the user code internal to the CPLD. It is intended that this clock will drive the logic of the user code.





The CPLD is responsible for asserting the PWR\_ENABLE signal to the oscillator. The signal must assert high for the oscillator to operate. The PWR\_ENABLE signal is available on the following CPLD pin:

Component	Net Name	Pin on CPLD	Signal in EPT Project Pinout
U10	PWR_ENABLE	99	10MHz_ENABLE

If the oscillator is not needed, de-assert the PWR\_ENABLE signal.

## 3.6 Digital I/Os

The BeeProLogic has one 8 pin header that provide 5 digital Inputs and Outputs. All of the I/O's are +3.3 VDC only. All I/O's connect directly from the CPLD.





The digital pins of the I/O Connector are directly accessible from pins on the CPLD. The user can access these pins by defining them in user HDL code. Then ensure that the pins are connected properly using the Pin Planner tool of Quartus.



Component	Net Name	Pin on CPLD	Signal in EPT
			Project Pinout
J7	FG_GPIO_1	41	USER_GP_1
J7	FG_GPIO_2	42	USER_GP_2
J7	FG_GPIO_3	47	USER_GP_3
J7	FG_GPIO_4	37	USER_GP_4
J7	FG_GPIO_5	38	USER_GP_5

All CPLD I/O are intrinsically bidirectional. Based on the I/O direction specified in the configuration file, each I/O can be configured as input-only, output-only, or bidirectional. While the output buffer of a bidirectional I/O has always included a dynamic output enable signal, MAX V CPLDs also include an input buffer enable/disable capability. When an input buffer is dynamically disabled, the buffer presents its last known state to the CPLD core fabric, so that no inputs inside the CPLD are left floating.



## 3.7 Analog I/O's

The BeeProLogic includes a single channel 8 bit DAC. The user can write any 8 bit digital value to the DAC and the associated analog voltage will appear on the output.



The DAC is directly connected to the CPLD. The communication path between CPLD and the 8 bit DAC is via SPI bus.



Component	Net Name	Pin on CPLD	Signal in EPT
			Project Pinout
U22	DAC_CS	61	DAC_CS
U22	DAC_SCLK	58	DAC_SCLK
U22	DAC_SDI	57	DAC_SDI
U22	DAC_LDAC	56	DAC_LDAC

A 20K $\Omega$  potentiometer is connected to the VREF pin. This varies the voltage applied to the VREF pin and provides amplitude control for the analog output voltage. The MCP4901 DAC



chip will convert any eight bit digital word into an analog voltage. The settling time for the chip is 4.5µseconds. The output analog voltage can reproduce a sine wave of approximately 800Hz.

The user code will include the library that provides the SPI communications. The MCP4901 device is designed to interface directly with the Serial Peripheral Interface (SPI) port, which is available on many microcontrollers and supports Mode 0,0 and Mode 1,1. Commands and data are sent to the device via the SDI pin, with data being clocked-in on the rising edge of SCK. The CS pin must be held low for the duration of a write command. The write command consists of 16 bits and is used to configure the DAC's control and data latches.

There are no registers to set and no registers to read from in the MCP4901. The chip has a maximum SPI clock frequency of:

#### • 5MHz

It requires to eight bit bytes to be written to the chip in order to perform a Digital to Analog conversion.

#### 3.8 Register Set

There is only one register accessible on the MCP4901, Write Command Register.

Bit	Bit	Bit	Bit	Bit	Bit	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
15	14	13	12	11	10										
0	BUF	GA	SHD N	D7	D6	D5	D4	D3	D2	D1	D0	Х	х	Х	Х

Where:

bit 15

0 = Write to DAC register

1 = Ignore this command

- bit 14 **BUF**: VREF Input Buffer Control bit
  - 1 = Buffered
  - 0 =Unbuffered
- bit 13 GA: Output Gain Selection bit

1 = 1x (VOUT = VREF \* D/256)

0 = 2x (VOUT = 2 \* VREF \* D/256)

- bit 12 SHDN: Output Shutdown Control bit
  - 1 = Active mode operation. VOUT is available.

0 = Shutdown the device. Analog output is not available. VOUT pin is connected to 500 k $\Omega$  (typical).

bit 11-0 D11:D0: DAC Input Data bits. Bit x is ignored.



#### 3.9 LEDs

The BeeProLogic includes eleven user LEDs. The LEDs are directly sinked from the CPLD with the cathode connected to +3.3V.



Component	Net Name	Pin on CPLD	Signal in EPT Project Pinout
D5	USER_LED_1	48	LED[0]
D6	USER_LED_2	40	LED[1]
D7	USER_LED_3	53	LED[2]
D8	USER_LED_4	54	LED[3]
D9	USER_LED_5	39	LED[4]



D10	USER_LED_6	36	LED[5]
D11	USER_LED_7	35	LED[6]
D12	USER_LED_8	69	LED[7]
D13	USER_LED_9	95	LED[8]
D14	USER_LED_10	96	LED[9]
D15	USER_LED_11	97	LED[10]

They use the +3.3V I/O's along with a 220 Ohm series resistor for each LED. This provides the following current through the LEDS.

$$I_{LED} = \frac{V_0 - V_F}{R}$$
$$I_{LED} = \frac{3.3V - 2.0V}{220}$$
$$I_{LED} = 5.9mA$$

The code to drive the LEDs is either zero (1'b0) or floating (1'bz). First, declare the LED as an output. In the example below, the vector LED is set to 'reg' because it is driven in an always block.



//*************************************	k
//* Module Declaration	
//*************************************	k

#### module EPT\_5M240\_AP\_S2\_Top (

input wire	CLK_10MHZ,
input wire	RST,
input wire	SW_USER_1,
input wire	SW_USER_2,
input wire	SW_USER_3,
input wire	SW_USER_4,
input wire	SW_USER_5,
input wire	SW_USER_6,
input wire	SW_USER_9,
input wire	PWR_ENABLE
output wire	PWR_KILL,
output reg [10:0]	LED
);	

To turn the selected LED on, set the signal equal to 1'b0. This will apply a ground to the cathode side of the LED and allow current to flow through the circuit turning the LED on. To turn the selected LED off, set the signal equal to 1'bz. This will float the cathode side of the LED and no current will flow through the LED.



```
//-----
// Set the LED outputs
//-----
always @ (posedge CLK 10MHZ or negedge RST)
begin
 if(!RST)
     LED <= 8'hz;
 else
 begin
   if(state[LOAD LEDS])
   begin
     if ( led reg[0] )
        LED[0] = 1'b0;
     else
        LED[0] = 1'bz;
     if ( led_reg[1] )
        LED[1] = 1'b0;
     else
        LED[1] = 1'bz;
     if ( led_reg[2] )
        LED[2] = 1'b0;
     else
        LED[2] = 1'bz;
```

## 3.10 Pushbutton Switches

The BeeProLogic includes eight push button switches. All are momentary contact switches. They include a 1uF cap to ground to debounce both switches. The code to use these switches is simple, just declare an input on the selected switch pin. Then use code to activate the a function with the input signal goes to low.







Component	Net Name	Pin on CPLD	Signal in EPT		
			<b>Project Pinout</b>		
SW1	SW_USER_1	53	SW_USER_1		
SW2	SW_USER_2	51	SW_USER_2		
SW3	SW_USER_3	50	SW_USER_3		
SW4	SW_USER_4	49	SW_USER_4		
SW5	SW_USER_5	34	SW_USER_5		
SW6	SW_USER_6	33	SW_USER_6		



	SW9	SW_USER_7	98	SW_USER_7
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#### 3.11 8 MBit Flash

The BeeProLogic includes an 8 Mbit Flash.



#### 3.12 Power Input

The BeeProLogic is designed to be operated from the following power source:

• Standard USB Micro-B cable

The board has a Molex style USB Micro-B connector on board. Connect the USB cable either to a USB Port on a PC or a standard charger (+5V @ 2A). This provides power for a high-efficiency switching regulator on-board to provide +3.3 VDC. The power supply provides reliable power under dynamic loads and high frequency switching internal to the CPLD.





## 3.13 JTAG Interface

Connector J7 on the rear of the board is the JTAG Connector. It is a JST 6x1 connector and the BeeProLogic includes an adapter to convert the 6x1 pins into the standard 5x2 JTAG Blaster connector.



This connector uses the standard Altera Blaster connector pinout.



The VCC(TRGT) is set to +3.3V on the BeeProLogic. There are no jumper settings to make in order to program the MAX V CPLD. Just connect a compatible Blaster to the connector and the PC, then use the Quartus software to program the CPLD.





# 4 Installing Quartus

You can download the Quartus Prime Lite by following the directions in the Section Downloading Quartus.

If you don't need to download Quartus, double click on the QuartusLiteSetup-xxx.xxx.wxwindows .exe (the xxx is the build number of the file, it is subject to change). The Quartus Prime Web Edition will start the installation process.







When the install shield window pops up click "Yes" or if needed, enter the administrator password for the users PC. Click "Ok"

Next, skip the "Download Quartus" section. Go down to the "Quartus Installer" section to complete the Quartus installation.

4.1.1 Downloading Quartus

The first thing to do in order build a project in Quartus is to download and install the application. You can find the latest version of Quartus at:

Intel FPGA Quartus Prime Lite

You will first need to apply for an account with Intel. Then use your login and password to access the download site. Click on the Download Windows Version.



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	Note: The Quartus Prime software is a full-feat download times may be lengthy.
	System Requirements
	Documentation Links
	Software Support

The file is 5.9 GB, so this could take a couple of hours depending on your internet connection. When download is complete, store the \*.tar file in a directory on your PC.



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Quartus Prime Lite Edition (Free)         Quartus Prime (indudes Nios II EDS) (9313MB)         Quartus Prime Help (508.4MB)         Devices         Arria II (536.5MB)         Cyclone IV (516.3MB)         Cyclone 10 LP (293.5MB)         Cyclone V (1434.3MB)         MAX II/V (13.1MB)         MAX 10 FPGA (360.3MB)         ModelSim - Intel FPGA Starter Edition (Free) (4318.8MB)         ModelSim - Intel FPGA Edition (4318.8MB)	Installs Arria II device support. (536.5MB)	
Instalibulider	< Back Next >	Cancel

Click "Next" to accept the defaults



🕥 Installing Quartus Prime Lite Edition (Free) 20.1.0.711	—		×
Ready to Install		in	tel
Summary: Installation directory: C:\intelFPGA_lite\20.1 Required disk space: 16760 MB Available disk space: 657864 MB			
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Wait for the installation to complete.







🕤 Installing Quartus Prime I	Lite Edition (Free) 20.1.0.711	-		×
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inter	Setup has finished installing Quartus Prime Lite Edition (Free) 20.1.0.711.  Launch USB Blaster II driver installation  Create shortcuts on Desktop  Launch Quartus Prime Lite Edition  Provide your feedback			
	< Back Fin	ish	Cano	cel

Click "Ok", then click "Finish". The Quartus Prime is now installed and ready to be used.



S Quartus Prime 20.1 Lite Edition X
Thank you for installing the Quartus Prime software - the #1 in performance and productivity. To upgrade to a full featured edition, please https://www.intel.com/content/www/us/en/products/programmable.html.
Select one of the following licensing options to continue:
Select one of the following options
O Buy a Quartus Prime software license
O Run the Quartus Prime software
O Add an IP license file (for users who have purchased IP)
OK Cancel

#### 4.1.3 Adding the EPT\_Blaster to Quartus Prime

Close out the Quartus Prime application. Locate the \Drivers\EPT\_Blaster folder on the EPT FPGA Development System DVD.



Follow these directions:

- 1. Open the C:\:\..\BEEPROLOGIC\_USB\_CPLD\_PROJECT\_x.x\_DVD  $DriversEPT_Blasterx64$  folder.
- 2. Select the file "jtag\_hw\_mbftdi\_blaster.dll" and copy it.
- 3. Browse over to C:\intelFPGA\_lite\xx.x\quartus\bin64.
- 4. Right click in the folder and select Paste



- 5. Click Ok.
- 6. Open the Quartus Prime application.

📙    😰 📙 🗢    C:\intelFPGA_lite\20.1\quartus\bin64				
File Home Share View				
← → < ↑ 📙 > This PC > Local Disk (C:) > intelFPGA_lite > 20.1 >	quartu	us → bin64		
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> 🔥 common		📧 jtagserver.exe	6/5/2020 3:44 PM	Application
> drivers	~	legality_lab.dll	6/5/2020 3:39 PM	Application exten

The DLL is installed and the JTAG server should recognize it. Go to the section "Programming the FPGA" of this manual for testing of the programming. If the driver is not found in the Programmer Tool->Hardware Setup box, see the JTAG DLL Insert to Quartus Prime Troubleshooting Guide.



# 5 Compiling, Synthesizing, and Programming CPLD



The CPLD on the BeeProLogic can be programmed with custom HDL code created by the user. Programming the CPLD requires the use of the Quartus Prime software and a standard JTAG Blaster. Once the user HDL code is written according to the syntax rules of the language (Verilog and VHDL) it can be compiled and synthesized using the Quartus Prime software. This manual will not focus on HDL coding or proper coding techniques, instead it will use the example code to compile, synthesize and program the CPLD.

## 5.1 Setting up the Project and Compiling

Once the HDL code (Verilog or VHDL) is written and verified using a simulator, a project can be created using Quartus Prime Lite. Writing the HDL code and simulating it will be covered in later sections. Bring up Quartus Prime Lite, then use Windows Explorer to browse to C:\Users\nelso\Documents to create a new directory called: "EPT\_5M240\_FG\_Blinky".





Create a folder called: EPT\_5M240\_FG\_Blinky\EPT\_5M240\_AP\_S2\_Top directory to store your project. Type in a name for your project "EPT\_5M240\_AP\_S2\_Top".



Open Quartus Prime by clicking on the icon





Under Quartus, Select File->New Project Wizard. The Wizard will walk you through setting up files and directories for your project.



0	Quartus Prime Lite Edition										
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6	Save All	Ctrl+Shift+S				(C:/Users/nelso/I	Documents/EPT_5	457_AP_M	14_Transfer_Tes	t/EPT_5M57_AF	P_M4_Trans
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At the Top-Level Entity page, browse to the C:\Users\<your name>\Documents\EPT\_5M240\_FG\_Blinky\EPT\_5M240\_AP\_S2\_Top directory to store your project. Type in a name for your project "EPT\_5M240\_AP\_S2\_Top".





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		te New Project Wizard	Device Family Cyclone TC
		Compartizione Bay Shawar Documentation Tenny Support Write Werkenberg New Project Wizard X	<ul> <li>Installed IP</li> <li>Project Directory</li> <li>No Selection Available</li> <li>Library</li> </ul>
		Directory, Name, Top-Level Entity What is the working directory for this project? biso/Documents/EPT_5M240_FG_Blinky/EPT_5M240_AP_S2_Top	<ul> <li>&gt; Basic Functions</li> <li>&gt; DSP</li> <li>&gt; Interface Protocols</li> <li>&gt; Memory Interfaces an</li> <li>&gt; Processors and Peripi</li> <li>&gt; University Program</li> </ul>
		EPT 5M240 AP S2 Top	Search for Partner IP
k	^	What is the name of the top-level design entity for this project? This name is case sensitive and must exactly match the entity name in the design file.	
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New Project Wizard			
Project Type			
Select the type of project to create.			
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O Project template			
Create a project from an existing design download design templates from the <u>De</u>	emplate. You can choose from sign Store.	design templates installed with the	e Quartus Prime software, or



Select Next. At the Add Files window: Browse to the  $Projects_HDL EPT_5M240_FG_Blinky$  folder of the BeeProLogicDevelopment System DVD. Copy the files from the following directory.

C:\Uolly\Code_FPGA\EPT_5M240_FG_Blinky\EPT_5M240_FG_Blinky Home Share View				
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Testbench	↑ □ Name	Date modified	Туре	Size
EPT_5M160_FG_Signal_Gen_Rev_1	FPT 5M240 AP S2 Top	12/5/2020 3:53 PM	File folder	
EPT_5M160_FG_Signal_Gen_Rev_2	ModelSim	2/20/2021 1:50 PM	File folder	
EPT_5M240_FG_Blinky	✓ I src	2/20/2021 1:50 PM	File folder	
EPT_5M240_FG_Blinky	🖂 📕 test	2/20/2021 1:50 PM	File folder	
EPT_5M240_AP_S2_Top	🖂 📜 Testbench	2/20/2021 1:50 PM	File folder	
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E Testbench				
EPT_5M240_FG_Blinky_Rev_1				
Then paste them in the C:\users\ <your r<br="">EPT_5M240_AP_S2_Top folder:</your>	name>\Documents\EP	T_5M240_FG_	Blinky	
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cdssetup	ModelSim	7/28/2023 11:03 AM	File folder	
he Contacts	📜 src	7/28/2023 11:03 AM	File folder	
📕 Cookies	est test	7/28/2023 11:03 AM	File folder	
Documents	Testbench	7/28/2023 11:03 AM	File folder	
EPT_5M57_AP_M4_Transfer_Test				
EPT_5M57_AP_U2_Transfer_Test				
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On the Add Files page, click the three "dots" button and navigate to the 'src' folder:

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	Specify the path names of a	any non-default libraries. Us	er Libraries					
			< Back Next >	Finish	Cancel	Help		
			Next >	1111311	cancer			

Select Next, at the Device Family group, select MAX V for Family. In the Available Devices group, browse down to 5M240ZT100C5 for Name.



imily, Device & Board	Settings				
Device Board					
elect the family and device you	want to target for compilat	ion.			
'ou can install additional device	support with the Install Dev	vices comr	nand on the Tools m	enu.	
o determine the version of the	Quartus Prime software in	which you	r target device is sup	ported, refer to the Device Support	List webpage.
Device family		Show in 'Available o	levices' list		
Family: MAX V		Daskager	A.m.(		
Device: All		Pin count: / Core speed grade: /	Any		
Target device			Any	•	
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Other: n/a			Show advanced	devices	
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Name	Core Voltage	LEs		UFM blocks	^
5M240ZT100C4	1.8V	240	1		
5M240ZT100C5	1.8V	240			
5M240ZT100I5	1.8V	240	1		
5M240ZT144C4	1.8V	240	1		
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Select Next, leave defaults for the EDA Tool Settings.



EDA tools:				
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Simulation	<none> -</none>	<none></none>	Run gate-level	simulation automatically afte
Formal Verification	<none></none>	]		
Board-Level	Timing	<none></none>	•	
	Symbol	<none></none>	•	
	Signal Integrity	<none></none>	•	
	Boundary Scan	<none></none>	•	

Select Next, then select Finish. You are done with the project level selections.



Summary	
When you click Finish, the project will be created	with the following settings:
Project directory:	C:/Users/nelso/Documents/EPT_5M240_FG_Blinky/EPT_5M240_AP_S2_Top
Project name:	EPT_5M240_AP_S2_Top
Top-level design entity:	EPT_5M240_AP_S2_Top
Number of files added:	4
Number of user libraries added:	0
Device assignments:	
Design template:	n/a
Family name:	MAX V
Device:	5M240ZT100C5
Board:	n/a
EDA tools:	
Design entry/synthesis:	<none> (<none>)</none></none>
Simulation:	<none> (<none>)</none></none>
Timing analysis:	0
Operating conditions:	
VCCINT voltage:	1.8V
Junction temperature range:	0-85 °C
	Deale Martin Fields Consel

Next, we will select the pins and synthesize the project.

## 5.1.1 Selecting Pins and Synthesizing

With the project created, we need to assign pins to the project. The signals defined in the top level file (in this case: EPT\_5M240\_AP\_S2\_Top.v) will connect directly to pins on the CPLD. The Pin Planner Tool from Quartus Prime will add the pins and check to verify that our pin selections do not violate any restrictions of the device. In the case of this example we will import pin assignments that created at an earlier time. Under Assignments, Select Import Assignments.



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Type ID Message Type I	Type 10 Message yes augments from other sources the Import Assignment dialog box, click the three dots button. mport Assignments acify the source and categories of assignments to import. aname: Copy existing assignments into EPT_5M240_AP_S2_Top.qsf.bak before importing OK Cancel Help	* All 🔕 🟡 🔥 💎 < <filter>:</filter>		💏 Find 😽 Find Next			
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 $Browse to the \Projects\_HDL \ EPT\_5M240\_FG\_Blinky \ EPT\_5M240\_AP\_S2\_Top folder of the BeeProLogicDevelopment System DVD. Select the "EPT\_5M240\_AP\_S2\_Top.qsf" file.$ 



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		Documents > EPT_5M240_FG_Blinky > EPT_5M240_AP_	_S2_Top >		
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	AppData	^ Name	Date modified	Туре	Size
	Application Data	db	7/28/2023 11:11 AM	File folder	
	cdssetup	incremental_db	7/28/2023 11:03 AM	File folder	
. Case	Contacts	output_files	7/28/2023 11:03 AM	File folder	
*	Cookies	EPT_5M240_AP_S2_Top.qsf	7/28/2023 11:11 AM	QSF File	4 KI
	Documents				
	EPT_5M57_AP_M4_Transfer_Test				
	EPT_5M57_AP_U2_Transfer_Test				
	EPT_5M240_FG_Blinky				
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Click Ok. Under Assignments, Select Pin Planner. Verify the pins have been imported correctly.





The pin locations should not need to be changed for BeeProLogicDevelopment System. However, if you need to change any pin location, just click on the "location" column for the particular node you wish to change. Then, select the new pin location from the drop down box.



eport		0099897969594	19 39 29 1 9 08 98 83 79 68 53 48 38 28 19 07 97 8	37776	Pin	Legend		
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dSKS		1850 1950 2050 - • •		1058 1057 1056	Ē	DEV (	DE	
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Named." Y & Edit				1/0 0 1	110.5		Fitter	Pins: all
Node Name	Direction	LO	cation	I/O Bank	I/O St	andard	eserve	Current Strengt
<ul> <li>LED[0]</li> </ul>	Unknown	PIN_69	2		3.3-V LVTTL	(default)		16mA (default)
<ul> <li>LED[1]</li> </ul>	Unknown	PIN_48	1		3.3-V LVTTL	(default)		16mA (default)
<ul> <li>LED[2]</li> </ul>	Unknown	PIN_40	1		3.3-V LVTTL	(default)		16mA (default)
<ul> <li>LED[3]</li> </ul>	Unknown	PIN_53	2		3.3-V LVTTL	(default)		16mA (default)
• LED[4]	Unknown	PIN_54	2		3.3-V LVTTL	(default)		16mA (default)
<ul> <li>LED[5]</li> <li>LED[5]</li> </ul>	Unknown	PIN_36	1		3.3-V LVTTL	(default)		16mA (default)
<ul> <li>LED[6]</li> <li>LED[7]</li> </ul>	Unknown	PIN_35	1		3.3-V LVTTL	(default)		16mA (default)
LED[7]	Unknown	PIN_39	1		3.3-V LVIIL	(default)		16mA (default)
LED[8]	Unknown	PIN_97	2		3.3-V LVTTL	(default)		16mA (default)
	Unknown	PIN_96	2		3.3-V LVTTL	(default)		16mA (default)
	Unknown	PIN_95	2		3.3-V LVIIL	(default)		16mA (default)
SW_USER_9	Unknown	PIN_98	2		3.3-V LVITL	(default)		16mA (default)
SW_USER 1	Unknown	PIN_49	2		3.3-V LVTTL	(default)		16mA (default)
SW USER 2	Unknown	PIN_51	1		3 3-V I VTTI	(default)		16mA (default)
SW USER 3	Unknown	PIN 50	1		3.3-V I VTTI	(default)		16mA (default)
SW USER 5	Unknown	PIN 34	1		3.3-V LVTTL	(default)		16mA (default)
SW USER 6	Unknown	PIN 33	1		3.3-V LVTTL	(default)		16mA (default)
◆ RST	Unknown	PIN_43	1		3.3-V LVTTL	(default)		16mA (default)
CLK_10MHZ	Unknown	PIN_12	1		3.3-V LVTTL	(default)		16mA (default)
CLK_32KHZ	Unknown	PIN_14	1		3.3-V LVTTL	(default)		16mA (default)
PWR_KILL	Unknown	PIN_83	2		3.3-V LVTTL	(default)		16mA (default)
PWR_ENABLE	Unknown	PIN_99	2		3.3-V LVTTL	(default)		16mA (default)
scnew node>>								

Exit the Pin Planner. Select the Start Compilation button.





Then compilation will start.



Quartus Prime Lite Edition - C:/Users/nelso/I	Documents/EPT_5M2	40_FG_Blinky/EPT_5M240	0_AP_S2_Top/EPT_5M240_AP_S2_To	p - EPT_5M240_AP_S2_Top		- 0	×
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Entity:Instance T MAX V: 5M240ZT100C5 #EPT_5M240_AP_S2_Top	able of Contents ** Flow Summary Flow Settings Flow Non-Defaul Flow Elapsed Tim Flow OS Summar	Flow Summary < <filter>&gt; Flow Status Quartus Prime Version Revision Name Top-level Entity Name</filter>	Flow Failed - Sat Jul 29 10:58:31 20.1.0 Build 711 06020 SJ Lite EPT_5M240_AP_S2_Top EPT_5M240_AP_S2_Top	2023 Edition	<ul> <li>Installed IP</li> <li>Project Directory No Selection Ava Library</li> <li>Basic Functions</li> <li>Dop</li> </ul>	ailable	×
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<ul> <li>Compile Design</li> <li>Analysis &amp; Synthesis</li> <li>Fitter (Place &amp; Route)</li> <li>Assumbler (Generate programm</li> <li>Timing Analysis</li> <li>EOA Netilist Writer</li> <li>Edit Settings</li> </ul>	¢ >				+ Add		
All • • • • • • • • • • • • • • • • • •		💏 Find 🖝 Fir	nd Next				
<ul> <li>Running Quartus Prim Command: quartus_map 16303Aggressive Area opti 18236Aumber of processors 20030Parallel compilation 12019Can't analyze file - 12019Can't analyze file -</li> </ul>	e Analysis & s read_settin mization mode has not been is enabled an - file src/EPJ - file src/Ifs - file src/fli d from "/src	synthesis gs_files=onww selected logi specified which d will use 4 of _SM240_AP_SZ_TOP (.v is missing ipflop.v is missi /mux.v" instead	ite_settings_files=off c area will be prioriti may cause overloading o the 4 processors detect .v is missing ng of from Quartus Prime m	EPT_5M240_AP_S2_Top -C EF zed at the potential cost n shared machines. Set t ed	rt_5M240_AP_S2_T c of reduced tin the global assig	op ning performar nment NUM_PAF	nce RAL →
System (4) Processing (20)							

If you forget to include a file or some other error you should expect to see a screen similar to this:



Quartus Prime Lite Edition - C:/Users/nelso	o/Documents/EPT_5M2	40_FG_Blinky/EPT_5M24	0_AP_S2_Top/EPT_5M240_AP_S2_Top - E	PT_5M240_AP_S2_Top	-	
File Edit View Project Assignments Proce	ssing Tools Window	Help			Sea	arch altera.com 🔍 🔍
🗋 🚾 🗟 🤟 🗊 🗊 つ 🤉 EPT_5M240_4	₽- ∠�\$\$\$  ▶	• ≁ ≮ Ҿ 🛇 & 🌺 🕻	9			
Project Navigator 🔺 Hierarchy 🔹 💷	Compilation Rep	port - EPT_5M240_AP_5	52_Top 🚨		P Catalog	
Entity:Instance MAX V: 5M240ZT100C5 #EPT_5M240_AP_S2_Top	Table of Contents ** Flow Summary Flow Settings Flow Non-Defaul Flow Elapsed Tim Flow OS Summar Flow OS Summary Flow Messages Flow Suppressed	Flow Stummary <pre>&amp; &lt;<filter>&gt; Flow Status Quartus Prime Version Revision Name Top-level Entty Name Family Device Timing Models</filter></pre>	Flow Failed - Sat Jul 29 10:58:31 202 20.1.0 Build 711 06020 SJ Lite Editi EPT_5M240_AP_52_Top EPT_5M240_AP_52_Top MAX V 5M240ZT100C5 Final	3 on		e oherals
Tasks Compilation Task Task Analysis & Synthesis Fitter (Place & Route) Timing Analysis EGA Netlist Writer Edit Settings					+ Add	
All O A A V < <filter>&gt;</filter>	•	💏 Find 🚿 Fin	nd Next			
<ul> <li>Too Dentity mux" obtain</li> <li>12021 Found 1 design unit</li> <li>1023 Found 1 design unit</li> <li>1023 Verilog HDL errors</li> <li>14001 Generated Suppresse</li> <li>Quartus Prime Analy</li> <li>230001 Quartus Prime Full</li> </ul>	ned from "/src including 1 is, including 1 is, including 1 is, including 1 it Net warning a at EPT_5M240_AP_ dd messages fild compilation was	<pre>c/mux.v" instead entities, in sou entities, in sou entities, in sou entities, in sou ut lfsr.v(31): cr .s2_Top.v(145): o c ://users/nelso/ s was unsuccessful. 3</pre>	of from Quartus Prime mega rce file /users/nelso/docu rce file /users/nelso/docu rce file /users/nelso/docu scated implicit net for "ne bject "RST_N" is not decla bocuments/terT_SM240_FG_Bli 1. 1 error, 7 warnings errors, 7 warnings	Function library ments/ept_5m240_fg_bli ments/ept_5m240_fg_bli ments/ept_5m240_fg_bli ments/ept_5m240_fg_bli red. verify the object wky/EPT_5M240_AP_S2_Top	hky/src/mux.v hky/src/lfsr.v hky/src/lipflop.v hky/src/ept_5m240_ name is correct. /output_files/EPT	(ap_s2_top.v If the name _5M240_AP_S2
System (4) Processing (20)						2% 00:00:10

Click on the "Processing" tab at bottom to see the error.



SQuartus Prime Lite Edition - C:/Users/nels	o/Documents/EPT_5M2	40_FG_Blinky/EPT_5M240	)_AP_S2_Top/EPT_5M240_AP_S2_Top	p - EPT_5M240_AP_S2_Top		- 0	×
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□	A- 1660 💷 🕨	***					
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	Flow Elapsed Tim	Revision Name	EPT_5M240_AP_S2_Top		V Library		
	Flow OS Summar	Top-level Entity Name	EPT_5M240_AP_S2_Top		> Dasic Functions		
	Flow Log	Family	MAXV		) Interface Brotocol	-	
	> Analysis & Synthe	Device	5M240ZT100C5		> Processors and D	arinharals	
	<ul> <li>Flow Messages</li> </ul>	Timing Models	Final		> University Progra	m	
	<ul> <li>Flow Suppressed</li> </ul>				<ul> <li>Search for Partner</li> </ul>	IP	
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S Curture (4)							,
System (4) Processing (20)							

The error in this case is the missing object "RST\_N". Go to the source file "EPT\_5M240\_AP\_S2\_Top.v", and open it in an editor.



Scroll down to the line, 145 and locate the object "RST\_N"..



-	T CAA	
ER	1_DMI	
135	- /	/**************************************
136		
137		assign button_register = {!SW_USER_1, !SW_USER_2, !SW_USER_3, !SW_USER_4, !SW_USER_5, !SW_USER_
138		
139		assign PWR_KILL = 1'b0;
140		
141	F	//
142		// 32KHz Timer
143	-	//
144		
145		always @ (posedge CLK_32KHZ or negedge RST_N)
146	9	begin
147		if(!RST)
148		timer_32khz <= 0;
149		else
150	P	begin
151		<pre>if(trigger_state &lt;= TRIGGER_RESET)</pre>
152	P	begin
153		timer_32khz <= 0;
154	1	end
155		else
156	P	begin
157		<pre>timer_32khz &lt;= timer_32khz + 1'dl;</pre>
158	-	end
159	-	end
160	1	end
100 100 100		

Chage the object to "RST". Click save then re-run the Compile process. After successful completion, the screen should look like the following:



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File Edit View Project Assignments Pl	ocessing Tools Window	нер		Search	altera.com
		*** <b>0</b> ***			
Project Navigator A Hierarchy	Compilation Rep	ort - EPT_5M240_AP_5	S2_Top	IP Catalog	N I
Entity:Instance	Table of Contents **	How Summary		×  ■ Installed IP	
MAX V: 5M240ZT100C5	Flow Summary	<<>>Itter>>		V Project Directory	
*EPT_5M240_AP_S2_Top	<ul> <li>Flow Settings</li> <li>Flow Non-Default</li> <li>Flow Elapsed Tim</li> <li>Flow Clapsed Tim</li> <li>Flow Cog</li> <li>Analysis &amp; Synth</li> <li>Fltter</li> <li>Flow Messages</li> <li>Flow Messages</li> <li>Flow Messages</li> <li>Flow Messages</li> <li>Flow Messages</li> <li>Timing Analyzer</li> </ul>	Flow Status Quartus Prime Version Revision Name Top-level Entity Name Family Device Timing Models Total logic elements Total pins Total virtual pins UFM blocks	Successful - Sat Jul 29 11:05:51 2023 20.10 Build 711 06020 SJ Lite Edition EPT_SM240_AP_S2_Top PAT_SM240_AP_S2_Top MAX V 5M240ZT100C5 Final 175 / 240 (73 %) 23 / 79 (29 %) 0 0 / / 1 (0 %)	No Selection Available Library Basic Functions DSP Interface Protocols Processors and Periphers University Program Search for Partner IP	als
Task       > Compile Design       > Analysis & Synthesis       > Fitter (Place & Route)       > EDA Netlist Writer       = Edit Settings	× < >			- Add	
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System (4) Processing (114)					

At this point the project has been successfully compiled, synthesized and a programming file has been produce. See the next section on how to program the CPLD.

# 5.1.2 Programming the CPLD

Programming the CPLD is quick and easy. All that is required is a standard USB Micro-B cable, JST Adapter board and the EPT\_Blaster Driver DLL. Connect the BeeProLogic to the PC, open up Quartus Prime, open the programmer tool, and click the Start button. To program the CPLD, follow the steps to install the USB Driver and the JTAG Driver Insert for Quartus Prime.





If the project created in the previous sections is not open, open it. Click on the Programmer button.

File Edit View Project Assignm	ents Proce	ssing Tools Window	Help			Search altera.com
□ □ □ □ 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	T_5M240_/	⊷ <b>∠                                   </b>	* * * • • • •	9		
Project Navigator 🔺 Hierarchy	- 38 - 1	Compilation Rep	ort - EPT_5M240_AP_S	i2_Top 🛛	IP Catalog	124
Entity:Instance MAX V: 5M240ZT100C5		Flow Summary     Flow Settings	Flow Summary <ul> <li>&lt;<filter>&gt;</filter></li> <li>Flow Status</li> </ul>	Successful - Sat Jul 29 11:05:51 2023	V® Installed IP VProject Direct	ory
*EPI_SM240_AP_S2_Top	,	Flow Non-Defaul     Flow Etapsed Tim     Flow OS Summer     Flow Log     Analysis & Synth     Fitter     Flow Messages     Flow Suppressed     Assembler     Fitting Analyzer	Quartus Prime Version Revision Name Top-level Entity Name Family Device Timing Models Total logic elements Total pins Total virtual pins UFM blocks	2010 Build 711 06.020 SJ Uhe Edition EPT_SM240_AP_S2_Top MAX V 8X42021100C5 Final 75/240(73 %) 23/79(29%) 0 0(110%)	No Selection V Library > Basic Function > DSP > Interface Pro > Processors > University Pr © Search for Par	Available ms nocols nof Peripherals rogram tner IP
Tasks Compilation Task ✓ ► Compile Design ✓ ► Analysis & Synthesis ✓ ► Fitter (Place & Route) ← Assembler (Generate pr	ogramm					
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AII • • • •	< <filter>&gt;</filter>		💏 Find 🕷 Fin	nd Next		
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00						

The Programmer Window will open up with the programming file selected. Click on the Hardware Setup button in the upper left corner.



Hardware Setup	o Hardwaro		Mode: ITAG		T Pro				
Enable real time ISP to a	llow background progra	amming (for MAX II and	MAX V devices)			gress.			
Start	File	Device	Checksum	Usercode	Program/ Configure	Verify	Blank- Check	Examine	Securit Bit
Juliu Stop									
Auto Detect									
💥 Delete									
10									
Add File									
Change File									. F
Change File			III						+
Add File Change File Add File Add Device			III						4
Add File Change File Save File Add Device			III					<u> </u>	4

The Hardware Setup Window will open. In the "Available hardware items", double click on "EPT-Blaster v1.0".



Hardware Setup							×
Hardware Settings	JTAG S	ettings					
Select a programmin; hardware setup appli	g hardwa es only to	re setup to the curr	to use when p ent programm	rogramming d ner window.	levices. T	his programming	
Currently selected ha	rdware:	EPT-JT	AG-Blaster v1.	0 (64) [MBUSB	9-0]	•	
Hardware frequency:						H	z
Available hardware	items						
Hardware EPT-JTAG-Blaster	Hardware EPT-JTAG-Blaster v1.0 (64)			Port MBUSB-0		Add Hardware Remove Hardware	
						Close	

If you successfully double clicked, the "Currently selected hardware:" dropdown box will show the "EPT-Blaster v1.0 (64) [MBUSB-0]".



	JTAG S	ettings			
ect a programmin dware setup appli	g hardwa es only to	re setup to the curre	o use wher nt progran	n programming devic nmer window.	es. This programming
rently selected ha	ardware:	EPT-JTA	G-Blaster	/1.0 (64) [MBUSB-0]	
duare fraguence		No Hard	ware		
rdware frequency:		EPT-JTA	G-Blaster	1.0 (64) [MBUSB-0]	
vailable hardware	items				
Hardware			Server	Port	Add Hardware
PT-JTAG-Blaster	v1.0 (64)		Local	MBUSB-0	
					Remove Hardware

Click on the Auto-Detect button. This will verify that the EPT-Blaster driver can connect with the BeeProLogic device.

	asing loois will	uow riep -v				S	earch altera	.com
Hardware Setup E	PT-Blaster v 1.3b [MBUS llow background progra	8-0] Mod smming (for MAX II and I	e: JTAG 1AX V devices)	•	Progress:			
Ma Start	File	Device	Checksum	Usercode	Program/ Configure	Verify	Blank- Check	Examine
Auto Detect								
X Delete								
Change File			m					
Add Device								
1 <sup>°</sup> <sup>th</sup> Up								



#### Select the 5M570 under "Device".

Programmer - C:/Users/nelso/Documents/EPT\_5M240\_FG\_Blinky/EPT\_5M240\_AP\_S2\_Top/EPT\_5M240\_AP\_S2\_Top - EPT\_5M240\_AP\_S2\_Top - [EPT\_5M240\_AP\_S2\_T... 

 File Edit View Processing Tools Window Help
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4 Hard	dware Setup	EPT-JTAG-Blaster v1.0 (64) [MBU	SB-0]		Mode: JTAG		- Progre
🗌 Enat	ble real-time IS	F to allow background programmir	ng when available				
** Starl		File	Device	Checksum	Usercode	Program/ Configure	Verify
🖷 Stop	output_files	/EPT_5M240_AP_S2_Top.pof	5M240ZT100	00174DE4	00174AEC		
uto De	CFM UFM					L L	
Delet							
dd Fil							
ange I							
Save F	<						
ld Dev							
t∾Up							

#### Click on the "Change File" button and browse to the output\_files folder.

Hardware Setup	EPT-JTAG-Blas	Select New Progr	amming File			>	< <mark>cessfi</mark>
Enable real-time I	SP to allow backg	Look in:	\Users\nelso\Documents\EPT_5M240	_FG_Blinky\EPT_5M240_AF	S2_Top	G O O I II 🗉	
Stari Stop to Delet ave F UFM UFM UFM UFM UFM UFM UFM UF	File s/EPT_5M240_AF	My Computer nelso	Name db incremental_db output_files	Size	Type File Folder File Folder File Folder	Date Modified 7/29/2023 11:05:54 AM 7/28/2023 11:03:06 AM 7/29/2023 11:05:53 AM	nii :cur Bit
		File name:	¢			Open	



Click on the EPT\_5M240\_AP\_S2\_Top.pof file to select it.

New Pro	gramming File		×
Look in:	C:\Users\nelso\Documents\EPT_5M240_FG	G_Blinky\EPT_5M240_AP_S2_Top\output_files	• 🗘 🗘 🚺 🗉 🔳
▶ My Computer ≹ nelso	Name	Size Type 7 KB pof File	Date Modified 7/29/2023 11:05:51 AM
	<		>
File name:			Open
Files of type: Pr	ogramming Files (*.sof *.pof *.jam *.jbc *.ekp	*.jic)	- Cancel

Click the Open button in the lower right corner.

Next, selet the checkbox under the "Program/Configure" of the Programmer Tool. The checkboxes for the CFM and UFM will be selected automatically.



- nurun	ware Setup	EPT-JTAG-Blaster v1.0 (64) [MBUS	iB-0]		Mode: JTAG		• Prog
🗌 Enab	le real-time IS	P to allow background programmin	g when available				
Start		File	Device	Checksum	Usercode	Program/ Configure	Verify
** Stop uto De Delet	output_files, CFM UFM	/EPT_5M240_AP_S2_Top.pof	5M240ZT100	00174DE4	00174AEC	त् <u>य</u> त	
dd Fil Inge I							
ave F	٢						
d Dev ™Up	_==→						
	TDO						

Click on the Start button to to start programming the CPLD. The Progress bar will indicate the progress of programming.

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Processing Tools Window Help							Sea	rch altera.co	m 🦻
. EPT-JTAG-Blaster v1.0 (64) [MBUSB-0]		Mo	de: JTAG		~	Progress	s: 📘	6%	
SP to allow background programming when a	ailable								
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When the programming is complete, the Progress bar will indicate success.

4 Hard	ware Setup EPT-JTAG-Blaster v1.0 (64) [MBUSB-0	]		Mode: JTAG		<ul> <li>Prog</li> </ul>	ress: 00% (	Succes	sfi
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At this point, the BeeProLogic is programmed and ready for use. To test that the CPLD is properly programmed, follow the next section to see the LEDs blink in a heart beat pattern.

#### 5.1.3 Sample Code Operation

Once the BeeProLogic is programmed, operate the sample code by pressing the SW2. The LEDs will blink in a heart beat pattern. Press SW3 to see a different pattern.

