BEEPROLOGIC

CPLD DEVELOPMENT SYSTEM

Data Sheet

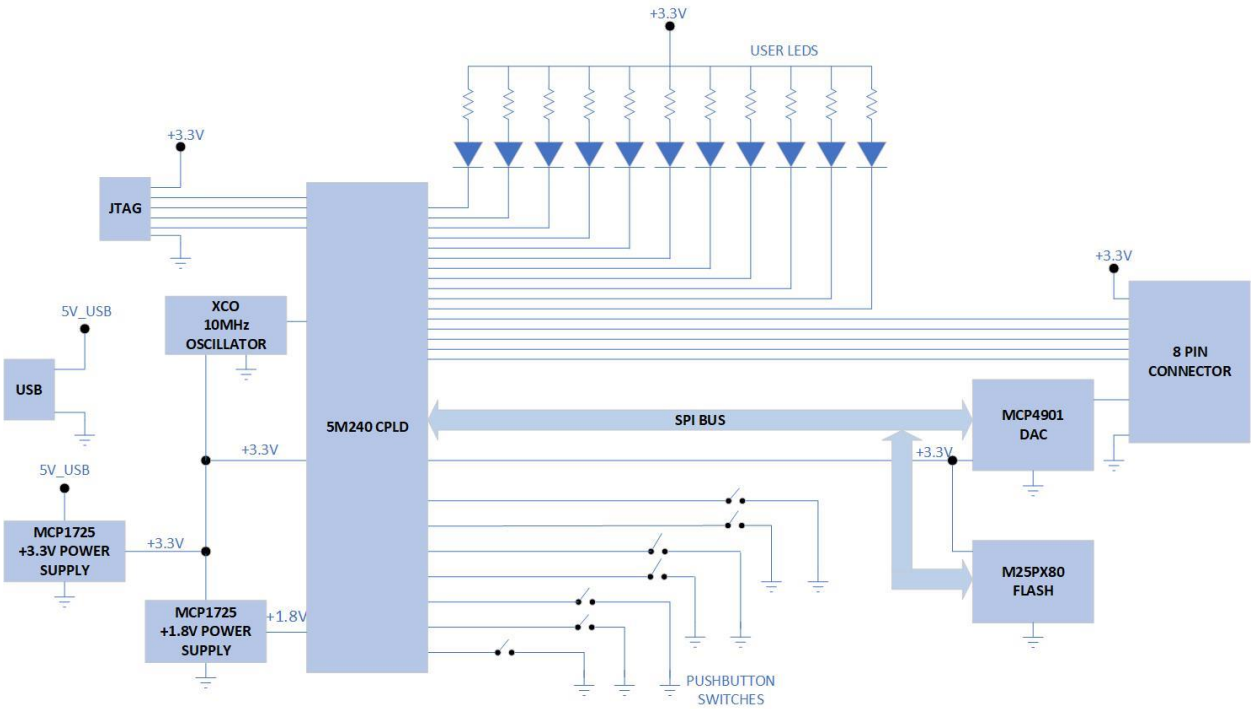
The BeeProLogic is a simplified CPLD development system. It allows the user to explore programmable logic with built in LEDs, Pushbuttons, Digital to Analog Converter and Flash on a single stand alone board.

The BeeProLogic board is equipped with an Intel 5M240 PLD; which is programmed using the Intel Quartus Prime software. The CPLD has 240 Logic Elements which is equivalent to 150

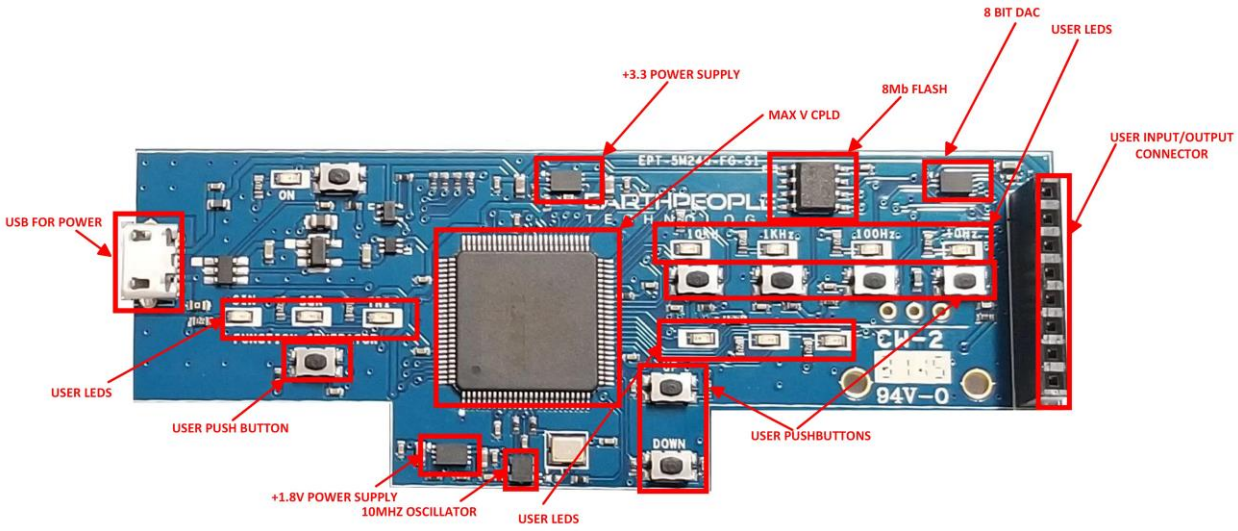
Macrocells. An on board 10 MHz oscillator provides all the timing for user code. The board also includes the following parts.

- Intel 5M240 in the TQFP 100 pin package
- 10 MHz oscillator
- 5 user Input/Outputs
- Eleven RGB LED's accessible by the user
- Seven Pushbutton switches accessible by the user
- 8 Bit DAC accessible using SPI Bus
- 4 Mbit Flash accessible using SPI Bus

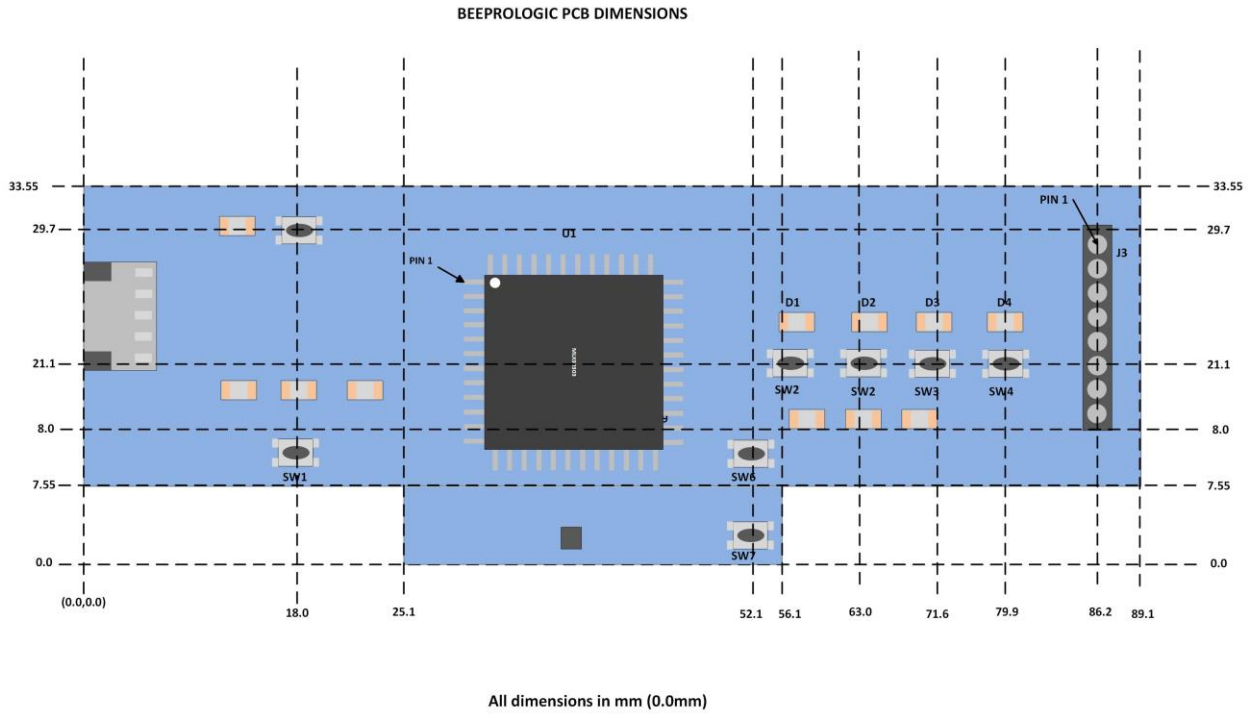
1 Block Diagram



User Manual CPLD Dev Sys For The BEE



2 Mechanical Dimensions



3 Pin Mapping

Pin Mapping between Connectors, MAXV CPLD and User code

J7 Connector

BeePrologic Connector-Pin #	BeePrologic Net Name	BeePrologic CPLD Pin Number	BeePrologic CPLD User Code Signal Name
J7-1	DAC_VOUT	NA	NA
J7-2	FG_GPIO_1	41	LB_COMM [1]
J7-3	FG_GPIO_2	42	LB_COMM [2]
J7-4	FG_GPIO_3	47	LB_COMM [3]
J7-5	FG_GPIO_4	37	LB_COMM [4]
J7-6	FG_GPIO_5	38	LB_COMM [5]
J7-7	+3.3V	NA	NA

J-8	GND	NA	NA

J6 Connector

BeeProlologic Connector-Pin #	**BeeProlologic Net Name**	**BeeProlologic CPLD Pin Number**	**BeeProlologic CPLD User Code Signal Name**
J6-1	+3.3V	NC	NC
J6-2	JTAG_TMS	22	TMS
J6-3	JTAG_TDI	23	TDI
J6-4	JTAG_TCK	24	TCK
J6-5	JTAG_TDO	25	TDO
J6-6	GND	NC	NC

Net Name Mapping between components

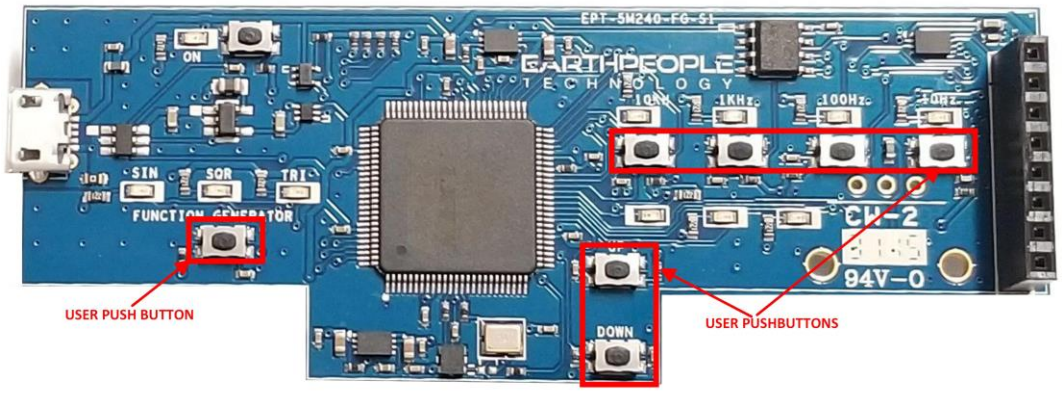
Component	**Pin**	**Net Name**	**Pin on CPLD**	**Signal in EPT Project Pinout**
10MHz Oscillator	3	GCLK1	12	CLK_10MHZ
Reset	NC	NA	43	RST
SW1	2	SW_USER_1	52	SW_USER_1
SW2	2	SW_USER_2	51	SW_USER_2
SW3	2	SW_USER_3	50	SW_USER_3
SW4	2	SW_USER_4	49	SW_USER_4
SW5	2	SW_USER_5	34	SW_USER_5
SW6	2	SW_USER_6	33	SW_USER_6
SW9	2	SW_USER_7	99	SW_USER_7
D8	1	LED_GR_1_N	54	LED[0]
D5	1	LED_GR_2_N	48	LED[1]
D6	1	LED_GR_3_N	40	LED[2]
D7	1	LED_GR_4_N	53	LED[3]
D12	1	LED_GR_5_N	69	LED[4]
D9	1	LED_GR_6_N	39	LED[5]
D10	1	LED_GR_7_N	36	LED[6]
D11	1	LED_GR_8_N	35	LED[7]

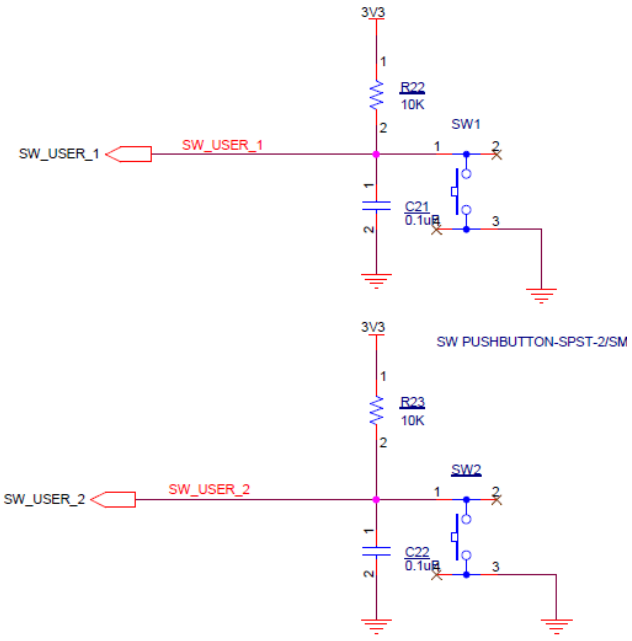
D13		LED_GR_9_N	95	LED[8]
D14		LED_GR_10_N	96	LED[9]
D15		LED_GR_11_N	97	LED[10]
U22	2	DAC_CS	61	DAC_CS
	3	DAC_SCLK	58	DAC_SCLK
	4	DAC_SDI	57	DAC_SDI
	5	DAC_LDAC	56	DAC_LDAC
U27	1	FLASH_CS	66	FLASH_CS
	6	DAC_SCLK	58	DAC_SCLK
	5	DAC_SDI	57	DAC_SDI
	1	FLASH_SDO	55	FLASH_SDO

4 Pushbutton switches

There are seven pushbutton switches on the BeeProLogic. All are momentary contact switches. They include a 1uF cap to ground to debounce both switches.

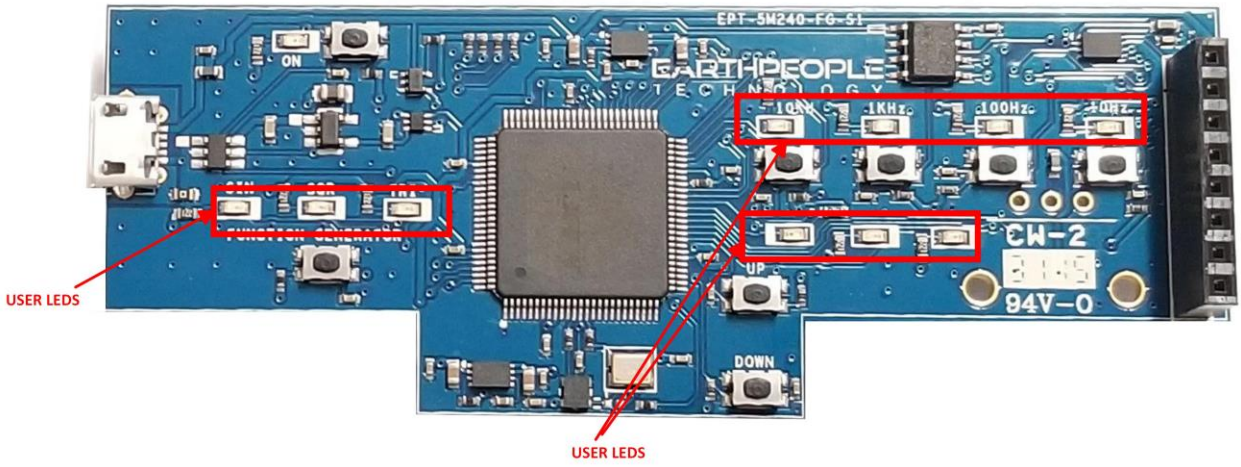
Component	Net Name	Pin on CPLD	Signal in EPT Project Pinout
SW1	SW_USER_1	52	SW_USER_1
SW2	SW_USER_2	51	SW_USER_2
SW3	SW_USER_3	50	SW_USER_3
SW4	SW_USER_4	49	SW_USER_4
SW5	SW_USER_5	85	SW_USER_5
SW6	SW_USER_6	30	SW_USER_6
SW9	SW_USER_7	27	SW_USER_7





4.1.1 User LEDs

The User LEDs are eleven Green LEDs. These LEDs are for use only with +3.3V.



Each series resistor uses a 220 Ohm in a resistor array. In order to light up the each LED, the user code must assert a zero on the associated signal for the LED. To turn off the LED, assert High Z on the signal. They use the +3.3V I/O's along with a 220 Ohm series resistor for each LED. This provides the following current through the LEDS

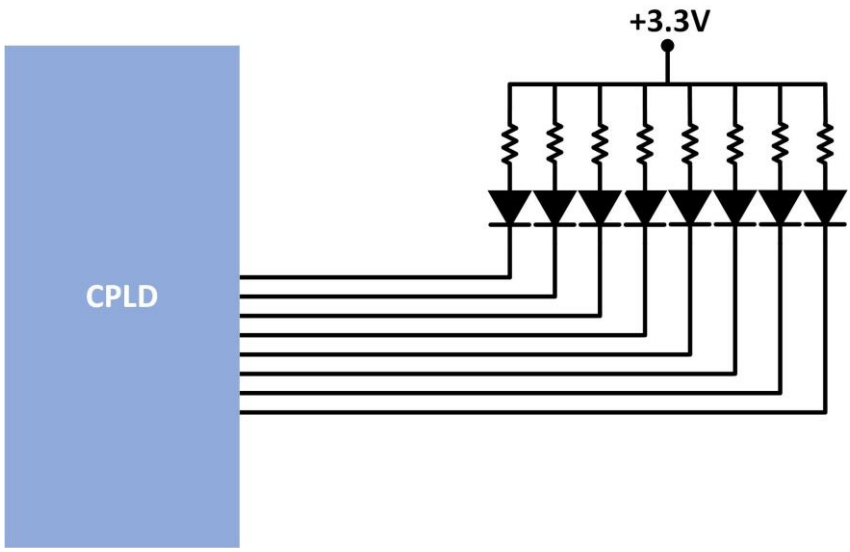
$$I_{LED} = \frac{V_O - V_F}{R}$$

$$I_{LED} = \frac{3.3V - 2.0V}{220}$$

$$I_{LED} = 5.9mA$$

The LED signals are organized on the following pins from the MAX V chip:

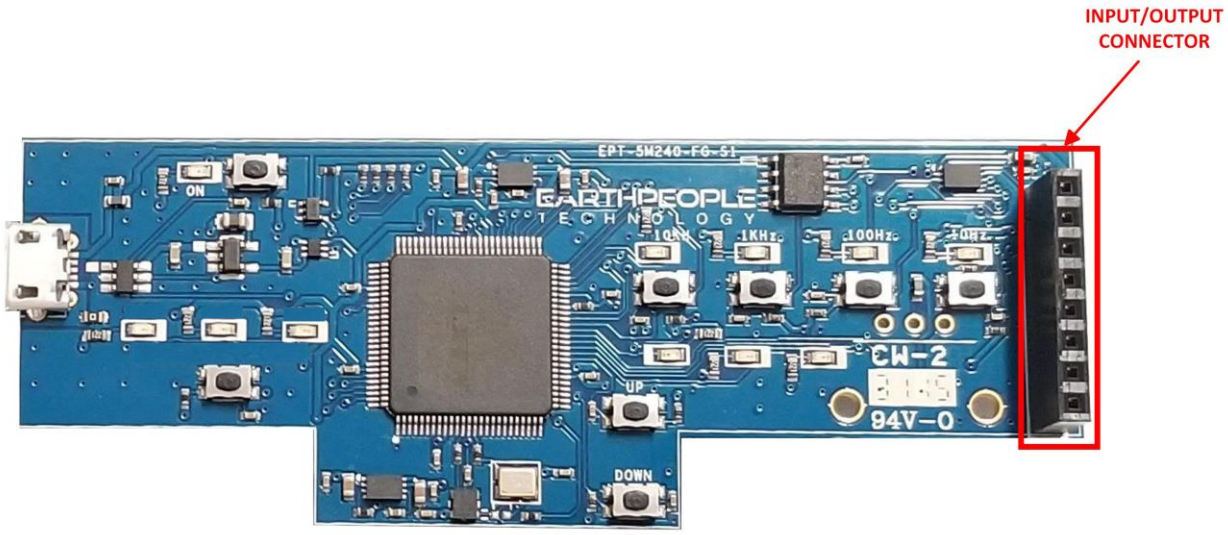
LED Number	Signal Name	MAX V Pin Number
D8	LED_GR_1_N	54
D5	LED_GR_2_N	48
D6	LED_GR_3_N	40
D7	LED_GR_4_N	53
D12	LED_GR_5_N	69
D9	LED_GR_6_N	39
D10	LED_GR_7_N	36
D11	LED_GR_8_N	35
D13	LED_GR_9_N	95
D14	LED_GR_10_N	96
D15	LED_GR_11_N	97



5 Inputs/Outputs

There are 5 General Purpose Inputs/Outputs available to the user. The user code can declare a pin to be input, output or tri-stated. The Pin Planner Tool under Quartus can be used to connect

the pin of the CPLD to the selected signal on the board.



Each I/O pin of the J7 connector is connected to a pin on the CPLD.

BeePrologic Connector-Pin #	BeePrologic Net Name	BeePrologic CPLD Pin Number	BeePrologic CPLD User Code Signal Name
J7-2	FG_GPIO_1	41	LB_COMM [1]
J7-3	FG_GPIO_2	42	LB_COMM [2]
J7-4	FG_GPIO_3	47	LB_COMM [3]
J7-5	FG_GPIO_4	37	LB_COMM [4]
J7-6	FG_GPIO_5	38	LB_COMM [5]

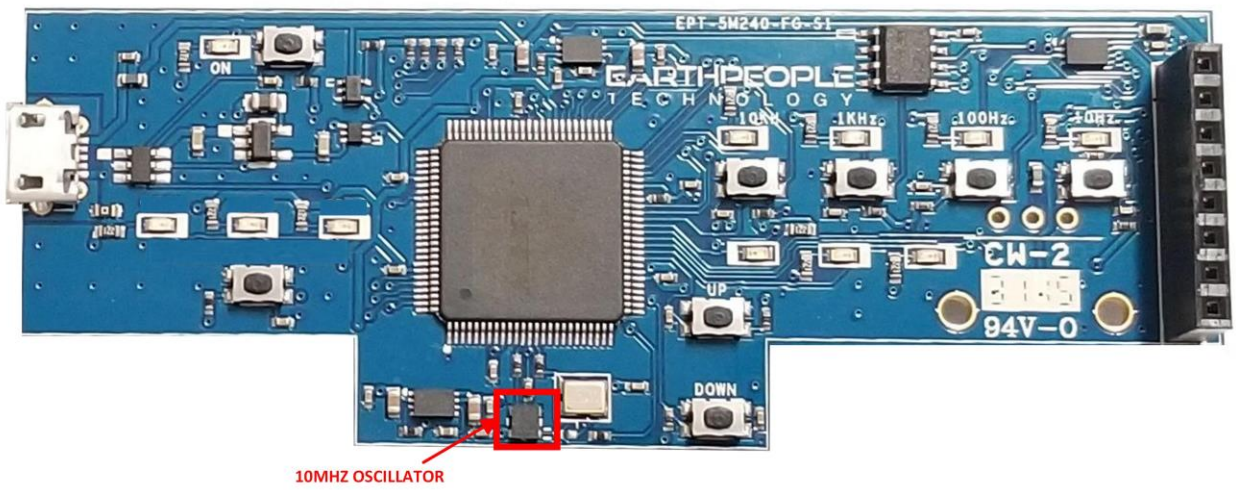
6 Oscillator

There is a 10MHz oscillator on the BeeProLogic, This oscillator has the following Vendor and P/N

- 10MHz, Renesas Electronics America Inc; P/N: ASDMB-10.000MHZ-LC-T

The oscillator is connected to the Global Clock input on the FPGA. The device provide stable clock for the CPLD's user code. The user can access the clock source by calling the net connected to the CPLD pin.

Component	Net Name	Pin on CPLD	Signal in EPT Project Pinout	
10MHz Osc	GCLK1	12	CLK_10MHZ	



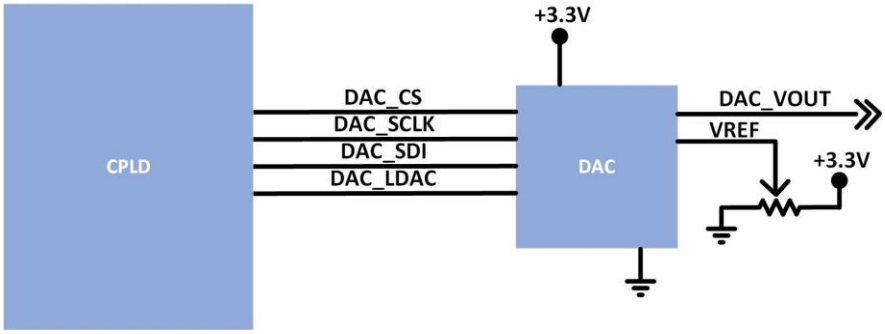
ASDMB-10.000MHZ-LC-T

PARAMETERS	MAX (unless otherwise noted)
Frequency	10MHz
Supply Voltage (VDD)	3.3V
Input Current (IDD) >9.900 ~ 10.100MHz	 25 mA
Standby Current	10 µA

Output Symmetry (50% VDD) >9.000 ~ 12.00MHz	 40% ~ 60%
Rise/Fall Time (10%/90% VDD Levels) (TR/TF) 1.000 ~ 15.000MHz	 6 nS
Output Voltage (VOL) (VOH)	10% VDD 90% VDD Min
Output Load (HCMOS)	15 pF
Start-up Time (TS)	10 mS
Frequency Stability	±25ppm
Operating Temperature	-40°C ~ 85°C

7 8 Bit Digital to Analog Converter

The BeeProLogic board features the MCP4091 Eight bit Digital to Analog chip. It is a single channel eight bit DAC. It includes a potentiometer which varies the voltage applied to the VREF pin of the DAC. This provides an amplitude control for the output of the DAC.



The SPI interface allows easy connection with an Arduino using the SPI library.

- 8 Bit DAC from MicroChip: MCP4901-E/MC

The device be can shut down by setting the Configuration Register bit. In Shutdown mode, most of the internal circuits are turned off for power savings, and the output amplifier is configured to

present a known high resistance output load (500 kΩ typical).

The device include double-buffered registers, allowing synchronous updates of the DAC output using the LDAC pin. These devices also incorporate a Power-on Reset (POR) circuit to ensure reliable powerup.

The device utilizes a resistive string architecture, with its inherent advantages of low Differential Non-Linearity (DNL) error and fast settling time. This device is specified over the extended temperature range (+125°C).

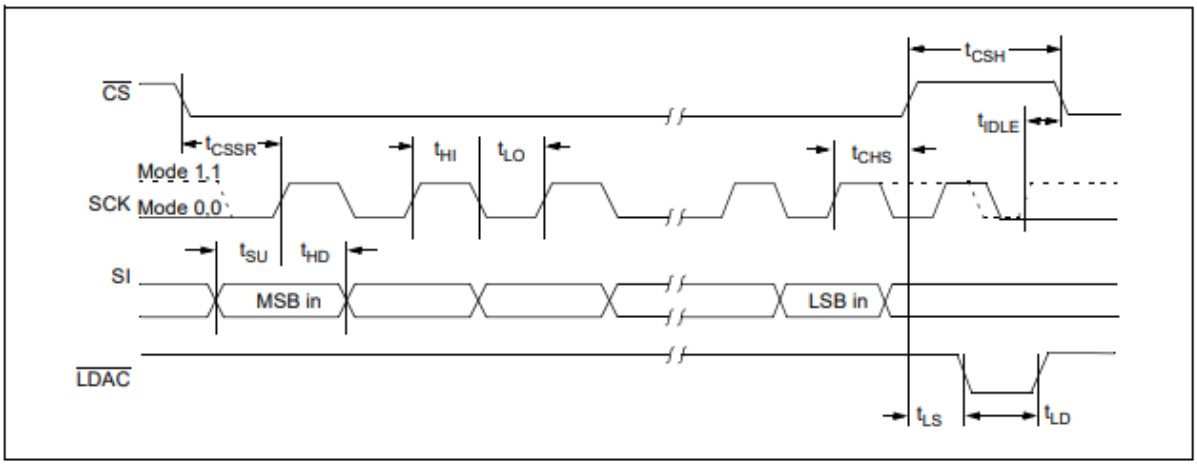
7.1.1 SPI Bus

The MCP4901 chip utilizes a 3-wire synchronous serial protocol to transfer the DAC's setup and output values from the digital source. The serial protocol can be interfaced to SPI or Microwire peripherals that are common on many microcontrollers. In addition to the three serial connections (CS, SCK and SDI), the LDAC pin synchronizes the analog output (VOUT) with the pin event. By bringing the LDAC pin down "low", the DAC input code and settings in the input register are latched into the output register, and the analog output is updated.

The MCP4901 chip is an SPI Slave. Any SPI host can communicate with the chip at speeds up to 20 MHz. The chip has no minimum SPI clock speed. The chip will respond to any SPI slave at any clock rate as long as it does not exceed 20 MHz. The table below displays the SPI parameters for the chip.

Parameters	Sym	Min	Typ	Max	Units
Clock Frequency	FCLK			20	MHz
Clock High Time	t_{HI}	15			ns
Clock Low Time	t_{LO}	15			ns
CS Fall to First Rising CLK Edge	t_{CSSR}	40			ns

Data Input Setup Time	t_{SU}	15			ns
Data Input Hold Time	t_{HD}	10			ns
SCK Rise to CS Rise Hold Time	t_{CHS}	15			ns
CS High Time	t_{CSH}	15			ns
LDAC Pulse Width	t_{LD}	100			ns
LDAC Setup Time	t_{LS}	40			ns
SCK Idle Time before CS Fall	t_{IDLE}	40			ns



7.1.2 LDAC Signal

The LDAC (latch DAC synchronization input) pin is used to transfer the input latch register to the DAC register (output latches, VOUT). When this pin is low, VOUT is updated with input register content. This pin can be tied to low (VSS) if the VOUT update is desired at the rising

edge of the CS pin. This pin can be driven by an external control device such as an MCU I/O pin.

7.1.3 Analog Output (VOUT)

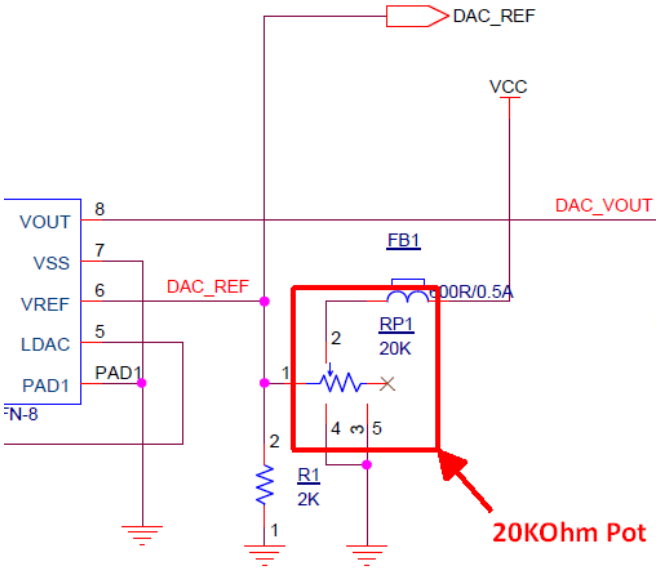
VOUT is the DAC analog output pin. The DAC output has an output amplifier. The full-scale range of the DAC output is from VSS to G*VREF, where G is the gain selection option (1x or 2x). The DAC analog output cannot go higher than the supply voltage (VDD).

7.1.4 Voltage Reference Input (VREF)

VREF is the voltage reference input for the device. The reference on this pin is utilized to set the reference voltage on the string DAC. The input voltage can range from VSS to VDD. This pin can be tied to VDD.

7.1.5 VREF Potentiometer

The EPT-4901-DA-S1 board includes a 20K potentiometer. This pot forms a voltage divider with a second resistor to vary the voltage applied to VREF. This varied voltage provides an amplitude control for the Analog Out voltage.



By varying the VREF, the accuracy of the DAC can be improved. This is because the analog

output step size between each DAC digital word is reduced. For example, if the VREF is set to 5V, the analog output step size is 5V/256 (Digital Steps) = 0.0195V per step. If the VREF is set to 2.5V, the analog output step size is 2.5V/256 (Digital Steps) = 0.00976V per step. The smaller the analog step size (or quanta), the more accurate the analog signal can be.

7.1.6 ANALOG OUTPUT VOLTAGE (VOUT)

The DAC input coding of these devices is straight binary. Equation 4-1 shows the DAC analog output voltage calculation.

$$V_{OUT} = \frac{(V_{REF} \times D_n)}{2^n} G$$

Where:

V_{REF}	=	External voltage reference
D_n	=	DAC input code
G	=	Gain Selection
	=	2 for <$\overline{GA}$> bit = 0
	=	1 for <$\overline{GA}$> bit = 1
n	=	DAC Resolution
	=	8 for MCP4901
	=	10 for MCP4911
	=	12 for MCP4912

MCP4901 (n = 8)

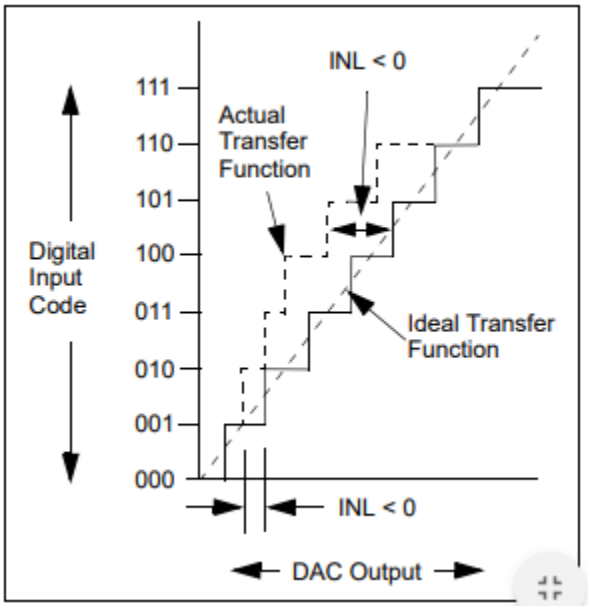
(a) 0V to 255/256*VREF when gain setting = 1x.

(b) 0V to 255/256*2*VREF when gain setting = 2x.

7.1.7 INL ACCURACY

Integral Non-Linearity (INL) error is the maximum deviation between an actual code transition point and its corresponding ideal transition point, after offset and gain errors have been removed. The two endpoints (from 0x000 and 0xFFF) method is used for the calculation. Figure 4-1 shows the details. A positive INL error represents transition(s) later than ideal. A negative INL error

represents transition(s) earlier than ideal.



7.1.8 OUTPUT AMPLIFIER

The DAC's output is buffered with a low-power, precision CMOS amplifier. This amplifier provides low offset voltage and low noise. The output stage enables the device to operate with output voltages close to the power supply rails. Refer to Section 1.0 "Electrical Characteristics" for the analog output voltage range and load conditions. In addition to resistive load driving capability, the amplifier will also drive high capacitive loads without oscillation. The amplifier's strong output allows VOUT to be used as a programmable voltage reference in a system. Selecting a gain of 2 reduces the bandwidth of the amplifier in Multiplying mode. Refer to Section 1.0 "Electrical Characteristics" for the Multiplying mode bandwidth for given load conditions. 4.2.1.1 Programmable Gain Block The rail-to-rail output amplifier has two configurable gain options: a gain of 1x (= 1) or a gain of 2x (= 0). The default value is a gain of 2x (= 0).

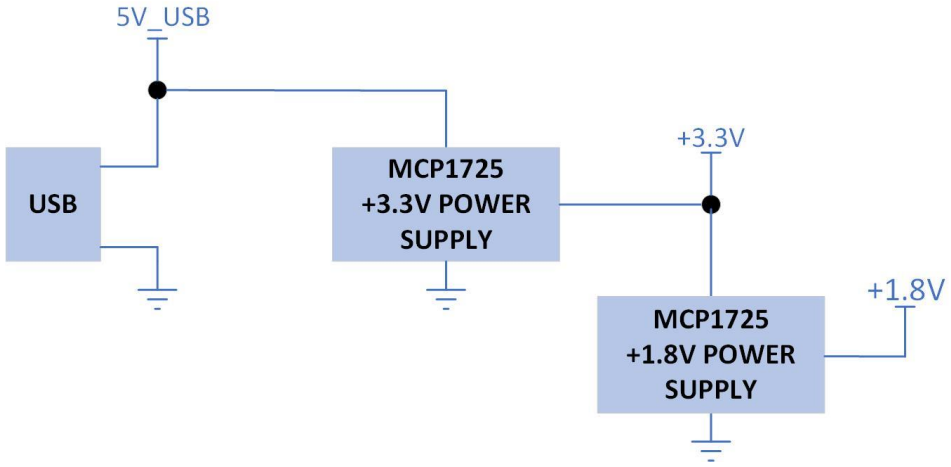
8 4Mbit Flash

The BeeProLogic includes a 4Mbit Flash chip.

- M25PX80-VMN6TP

9 BeeProLogic Power

The BeeProLogic can be powered from the USB bus of a Host/PC or the optional barrel connector. The USB supplies a maximum of +5V @ 500mA's. The components of the BeeProLogic must share this power with the user code that will run inside the CPLD along with any external power use.



9.1 Core Board Power Budget

Device	Part Number	+1.8V Power	+3.3V Power
CPLD	5M240	??? Defined by user code. EPT-Transfer-Demo code: 50mA	??? Defined by user code. . EPT-Transfer-Demo code: 50mA
4Mbit Flash	M25PX80-VMN6TP		
8Bit DAC	MCP4901-E/MC		2 mA (write current) 1 mA (read current)

10MHz Oscillator	CB3LV-3I-66M0		10 mA
User LEDs			550 mA
Total		**50mA**	**705.5mA**

*Theoritical Values only. This data needs to be validated

9.2 Core Board VUSB Power Budget

Device	**Part Number**	**VUSB**		
+1.8V Power Supply	MCP1725-1802E	70mA		
+3.3V Power Supply	MCP1725-3302E	815mA		
Total		**885mA**		

* Theoritical Values only. This data needs to be validated