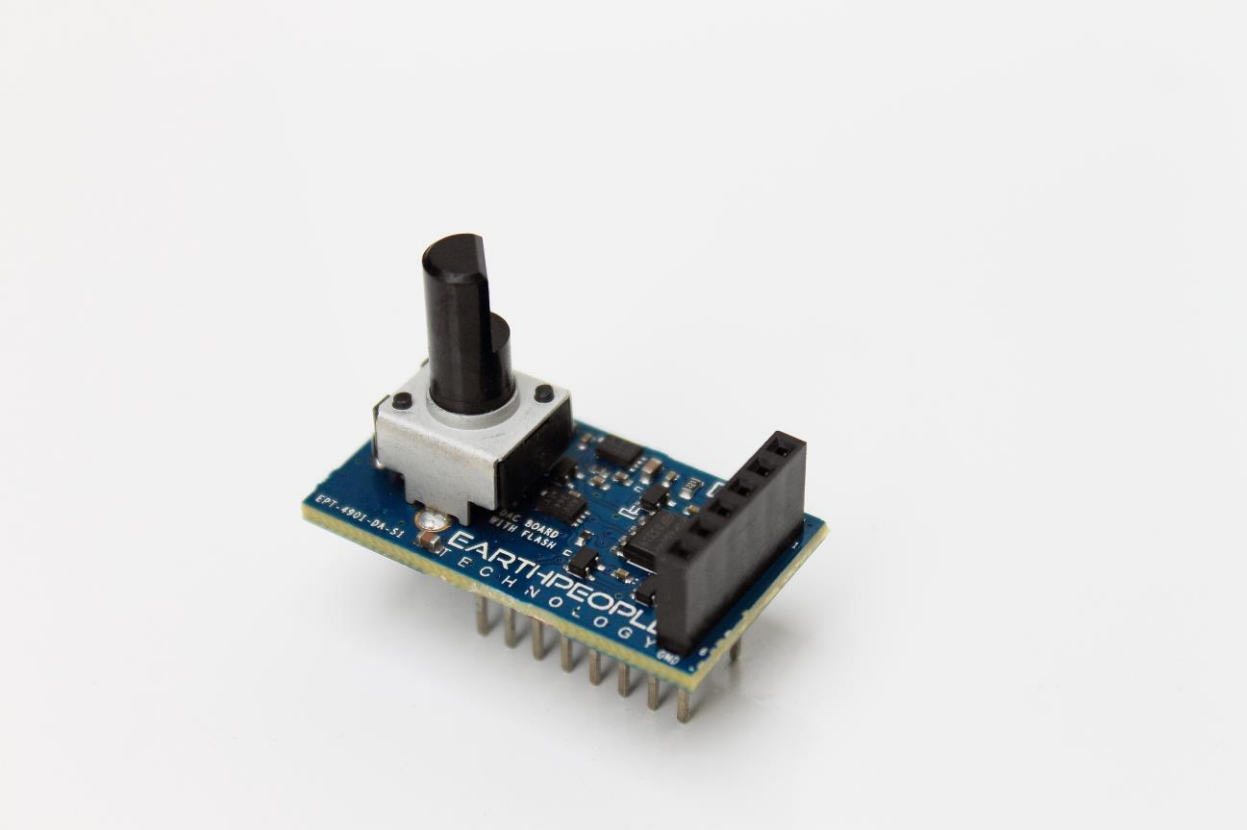
Digital To Analog Converter Board

EPT-4901-DA-S1

MCP4901 8 Bit Digital To Analog Converter Board

Data Sheet



This DAC board features the MCP4091 Eight bit Digital to Analog chip. It is designed to fit into a bread board and connect to any Arduino board. The chip operates from a single 2.7V to 5.5V supply with an SPI compatible Serial Peripheral Interface. So, it can accommodate the +3.3V and +5V Arduinos such as the Mini, Mini Pro, Nano.

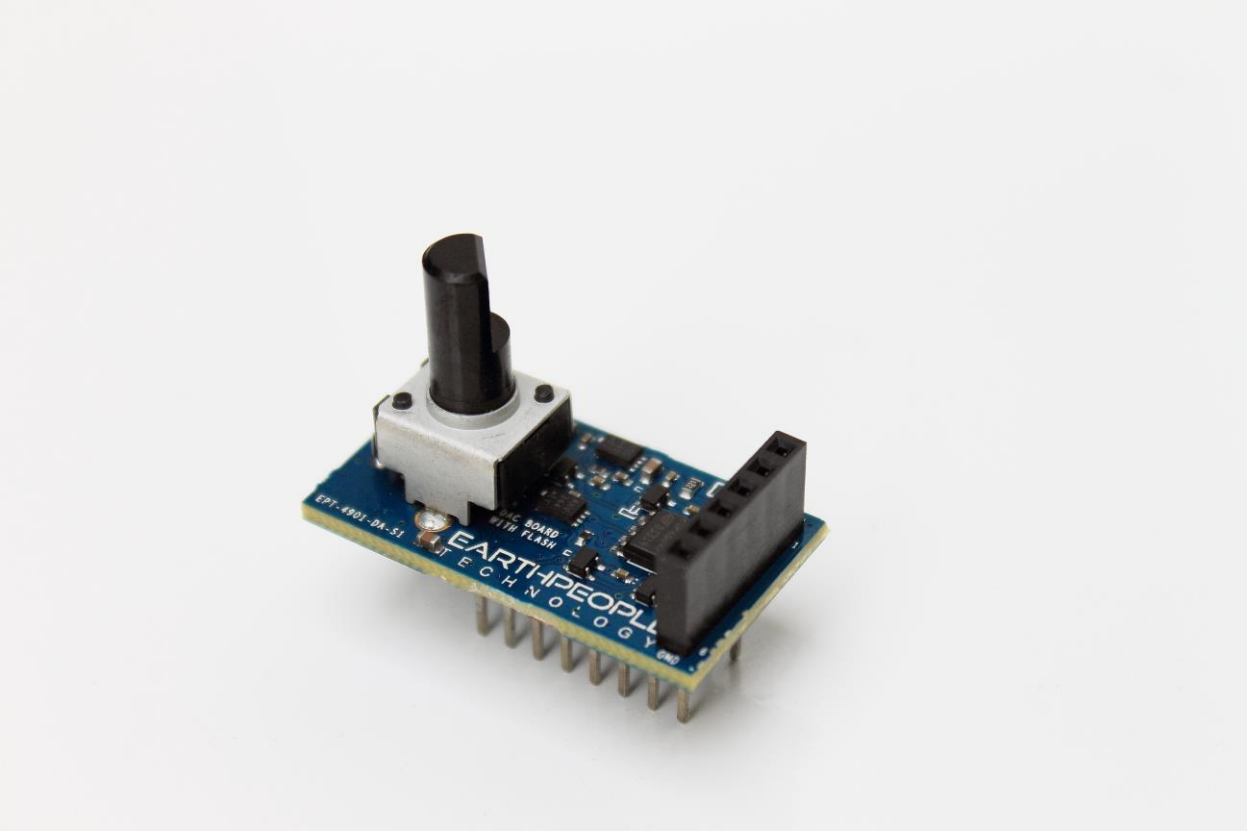
The EPT-4901-DA-S1 is a single channel eight bit DAC. It includes a potentiometer which varies the voltage applied to the VREF pin of the DAC. This provides an amplitude control for the output of the DAC. The SPI interface allows easy connection with an Arduino using the SPI library. There is a power indicator Green LED to indicate the board is powered. It has Headers that are surface mounted on the bottom of the board. Access to the SPI bus is made using these header pins. The DAC output is available on the under board headers or the top facing header. The board also includes a 8Mb Flash chip which utilized only in the +5V mode.

Hardware Features:

- Uses the SPI interface accessible by Arduino Libraries
- 8-bit, Rail to Rail, Voltage Output DAC
- Fast Settling Time of 4.5 µs
- Compatible with +3.3V or +5V interface
- 8Mb Flash chip utilized in +5V mode only

1 Description

The EPT-4901-DA-S1 contains a MCP4091 DAC chip. The board can be used to generate any analog voltage from ground to VREF. VREF is determined by a voltage divider using a potentiometer. The potentiometer allows VREF to vary from zero volts to VCC. VCC is determined by the voltage used to power the EPT-4901-DA-S1. The DAC will accept any input digital value from zero to 255 and convert this value to analog. However, VREF determines the step size of each digital value.



The EPT-4901-DA-S1 is compatible with the following Arduino Boards:

- Mini
- Mini Pro
- Nano
- Zero
- Uno
- Leonardo
- Pro

1.1 Hardware Description

The EPT-4901-DA-S1 consists of the following hardware

- MCP4901 Eight Bit DAC
- 20K Potentiometer for adjusting VREF
- One Green LED for power indication
- Breadboard Headers, SMT mounted
- Top Mounted Header

- 8Mb Flash for 5V use only

1.1.1 Digital to Analog Converter

The MCP4901 is a single channel 8-bit buffered voltage output Digital-to-Analog Converter (DAC). The devices operate from a single 2.7V to 5.5V supply with an SPI compatible Serial Peripheral Interface. The user can configure the full-scale range of the device to be VREF or 2*VREF by setting the gain selection option bit (gain of 1 of 2).

The device be can shut down by setting the Configuration Register bit. In Shutdown mode, most of the internal circuits are turned off for power savings, and the output amplifier is configured to present a known high resistance output load (500 kΩ typical).

The device include double-buffered registers, allowing synchronous updates of the DAC output using the LDAC pin. These devices also incorporate a Power-on Reset (POR) circuit to ensure reliable powerup.

The device utilizes a resistive string architecture, with its inherent advantages of low Differential Non-Linearity (DNL) error and fast settling time. This device is specified over the extended temperature range (+125°C).

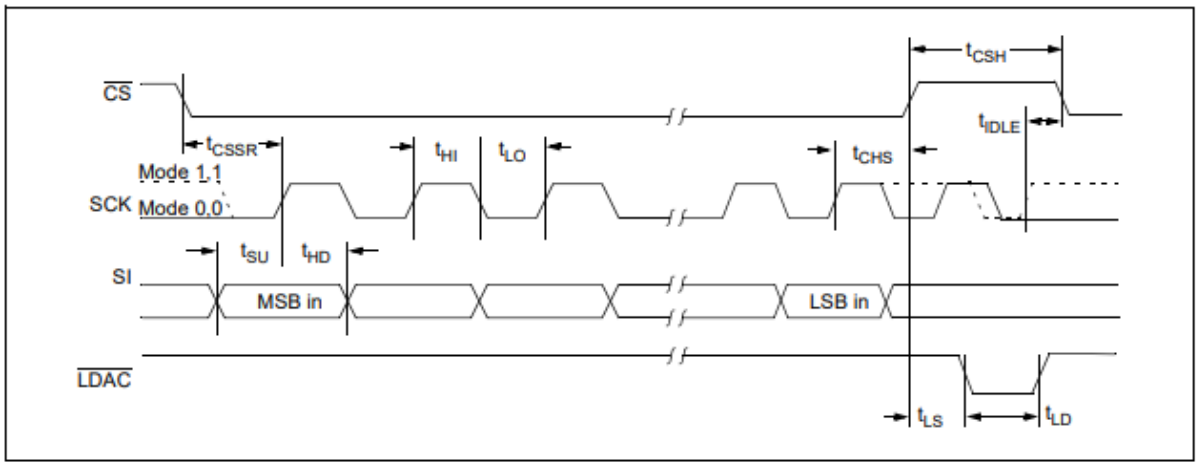
1.1.2 SPI Bus

The MCP4901 chip utilizes a 3-wire synchronous serial protocol to transfer the DAC's setup and output values from the digital source. The serial protocol can be interfaced to SPI or Microwire peripherals that are common on many microcontrollers. In addition to the three serial connections (CS, SCK and SDI), the LDAC pin synchronizes the analog output (VOUT) with the pin event. By bringing the LDAC pin down "low", the DAC input code and settings in the input register are latched into the output register, and the analog output is updated.

The MCP4901 chip is an SPI Slave. Any SPI host can communicate with the chip at speeds up to 20 MHz. The chip has no minimum SPI clock speed. The chip will respond to any SPI slave at any clock rate as long as it does not exceed 20 MHz. The table below displays the SPI parameters for the chip.

Parameters	Sym	Min	Typ	Max	Units

Clock Frequency	FCLK			20	MHz
Clock High Time	t_{HI}	15			ns
Clock Low Time	t_{LO}	15			ns
CS Fall to First Rising CLK Edge	t_{CSSR}	40			ns
Data Input Setup Time	t_{SU}	15			ns
Data Input Hold Time	t_{HD}	10			ns
SCK Rise to CS Rise Hold Time	t_{CHS}	15			ns
CS High Time	t_{CSH}	15			ns
LDAC Pulse Width	t_{LD}	100			ns
LDAC Setup Time	t_{LS}	40			ns
SCK Idle Time before CS Fall	t_{IDLE}	40			ns



1.1.3 LDAC Signal

The LDAC (latch DAC synchronization input) pin is used to transfer the input latch register to the DAC register (output latches, VOUT). When this pin is low, VOUT is updated with input register content. This pin can be tied to low (VSS) if the VOUT update is desired at the rising edge of the CS pin. This pin can be driven by an external control device such as an MCU I/O pin.

1.1.4 Analog Output (VOUT)

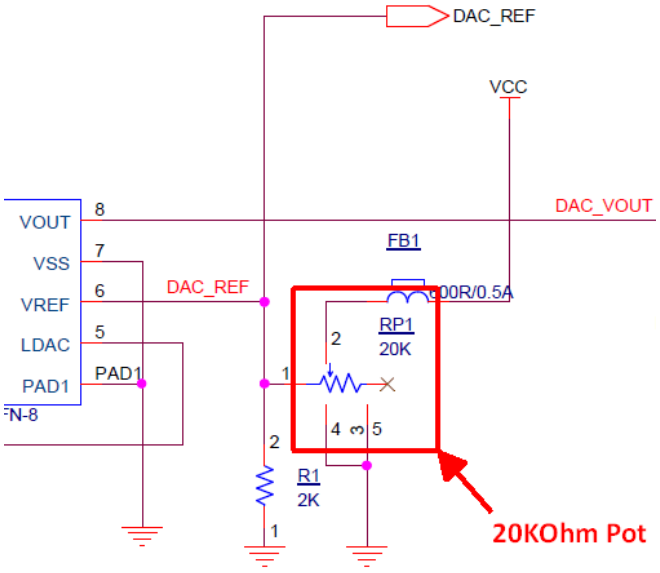
VOUT is the DAC analog output pin. The DAC output has an output amplifier. The full-scale range of the DAC output is from VSS to G*VREF, where G is the gain selection option (1x or 2x). The DAC analog output cannot go higher than the supply voltage (VDD).

1.1.5 Voltage Reference Input (VREF)

VREF is the voltage reference input for the device. The reference on this pin is utilized to set the reference voltage on the string DAC. The input voltage can range from VSS to VDD. This pin can be tied to VDD.

1.1.6 VREF Potentiometer

The EPT-4901-DA-S1 board includes a 20K potentiometer. This pot forms a voltage divider with a second resistor to vary the voltage applied to VREF. This varied voltage provides an amplitude control for the Analog Out voltage.



By varying the VREF, the accuracy of the DAC can be improved. This is because the analog output step size between each DAC digital word is reduced. For example, if the VREF is set to 5V, the analog output step size is 5V/256 (Digital Steps) = 0.0195V per step. If the VREF is set to 2.5V, the analog output step size is 2.5V/256 (Digital Steps) = 0.00976V per step. The smaller the analog step size (or quanta), the more accurate the analog signal can be.

1.1.7 ANALOG OUTPUT VOLTAGE (VOUT)

The DAC input coding of these devices is straight binary. Equation 4-1 shows the DAC analog output voltage calculation.

$$V_{OUT} = \frac{(V_{REF} \times D_n)}{2^n} G$$

Where:

V_{REF}	=	External voltage reference
D_n	=	DAC input code
G	=	Gain Selection
	=	2 for <$\overline{GA}$> bit = 0
	=	1 for <$\overline{GA}$> bit = 1
n	=	DAC Resolution
	=	8 for MCP4901
	=	10 for MCP4911
	=	12 for MCP4912

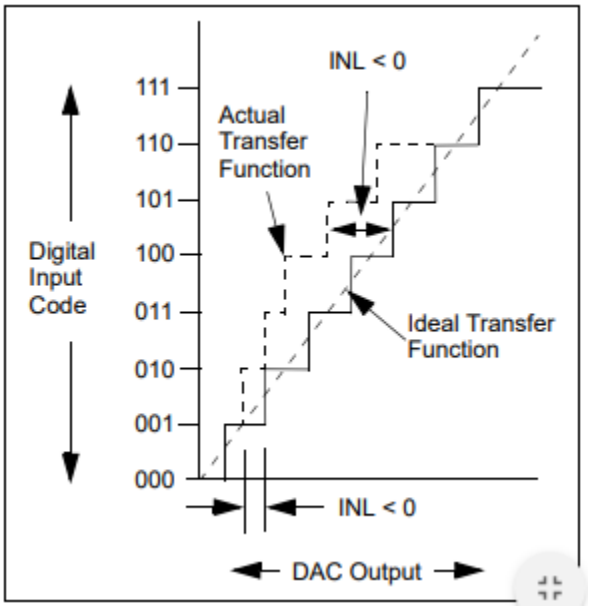
MCP4901 (n = 8)

(a) 0V to 255/256*VREF when gain setting = 1x.

(b) 0V to 255/256*2*VREF when gain setting = 2x.

1.1.8 INL ACCURACY

Integral Non-Linearity (INL) error is the maximum deviation between an actual code transition point and its corresponding ideal transition point, after offset and gain errors have been removed. The two endpoints (from 0x000 and 0xFFF) method is used for the calculation. Figure 4-1 shows the details. A positive INL error represents transition(s) later than ideal. A negative INL error represents transition(s) earlier than ideal.



1.1.9 OUTPUT AMPLIFIER

The DAC's output is buffered with a low-power, precision CMOS amplifier. This amplifier provides low offset voltage and low noise. The output stage enables the device to operate with output voltages close to the power supply rails. Refer to Section 1.0 "Electrical Characteristics" for the analog output voltage range and load conditions. In addition to resistive load driving capability, the amplifier will also drive high capacitive loads without oscillation. The amplifier's strong output allows VOUT to be used as a programmable voltage reference in a system. Selecting a gain of 2 reduces the bandwidth of the amplifier in Multiplying mode. Refer to Section 1.0 "Electrical Characteristics" for the Multiplying mode bandwidth for given load conditions. 4.2.1.1 Programmable Gain Block The rail-to-rail output amplifier has two configurable gain options: a gain of 1x (= 1) or a gain of 2x (= 0). The default value is a gain of 2x (= 0).

2 SERIAL INTERFACE

The MCP4901 chip is designed to interface directly with the Serial Peripheral Interface (SPI) port, which is available on many microcontrollers and supports Mode 0,0 and Mode 1,1.

Commands and data are sent to the device via the SDI pin, with data being clocked-in on the rising edge of SCK. The communications are unidirectional, thus the data cannot be read out of the MCP4901. The CS pin must be held low for the duration of a write command. The write command consists of 16 bits and is used to configure the DAC's control and data latches

2.1 *Register Set*

There is only one register accessible on the MCP4901, Write Command Register.

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	BUF	GA	SHDN	D7	D6	D5	D4	D3	D2	D1	D0	X	X	X	X

Where:

bit 15

0 = Write to DAC register
1 = Ignore this command

bit 14 **BUF**: VREF Input Buffer Control bit

1 = Buffered
0 = Unbuffered

bit 13 **GA**: Output Gain Selection bit

1 = 1x (VOUT = VREF * D/256)
0 = 2x (VOUT = 2 * VREF * D/256)

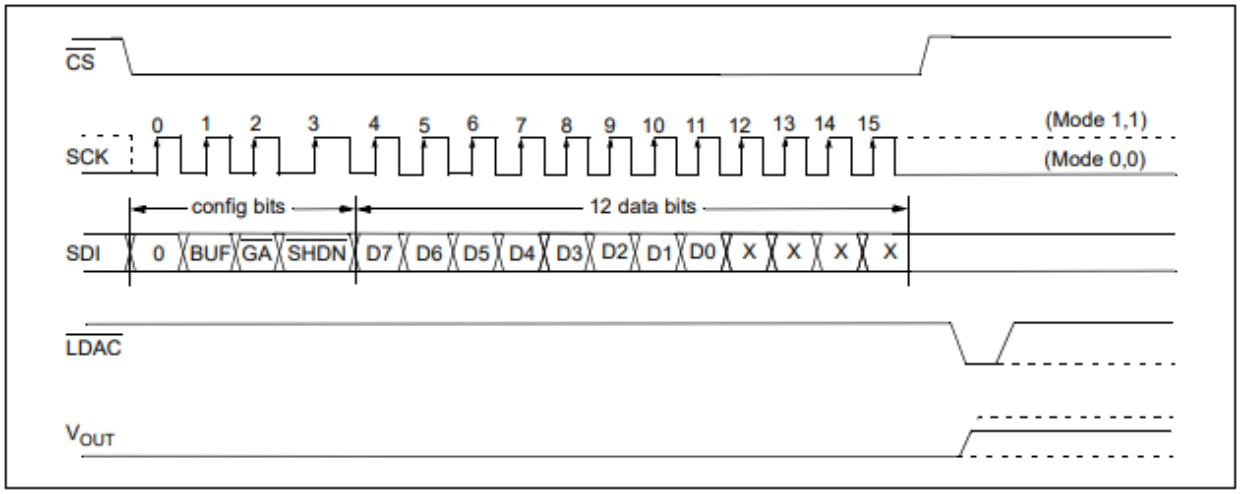
bit 12 **SHDN**: Output Shutdown Control bit

1 = Active mode operation. VOUT is available.
0 = Shutdown the device. Analog output is not available. VOUT pin is connected to 500 kΩ (typical).

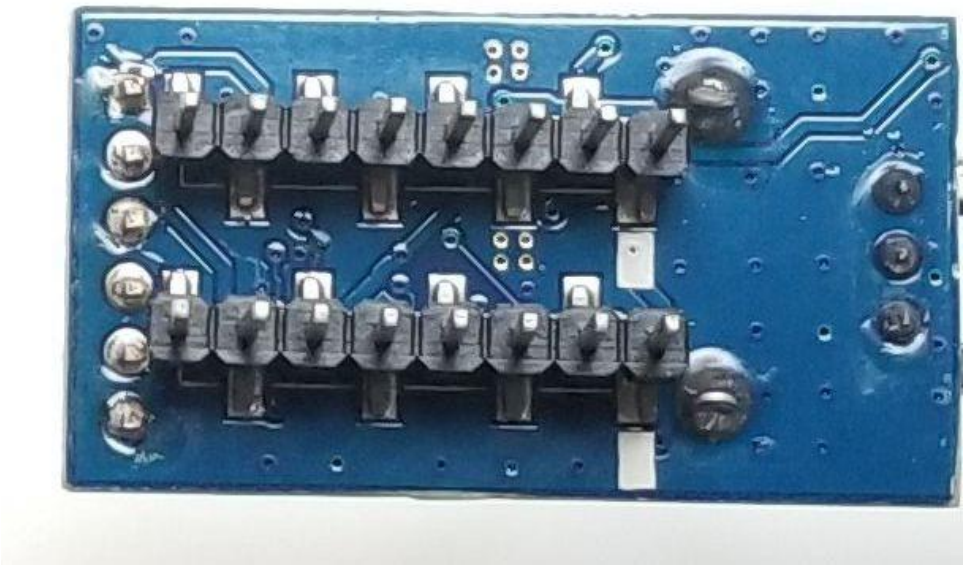
bit 11-0 D11:D0: DAC Input Data bits. Bit x is ignored.

2.2 *Write Command*

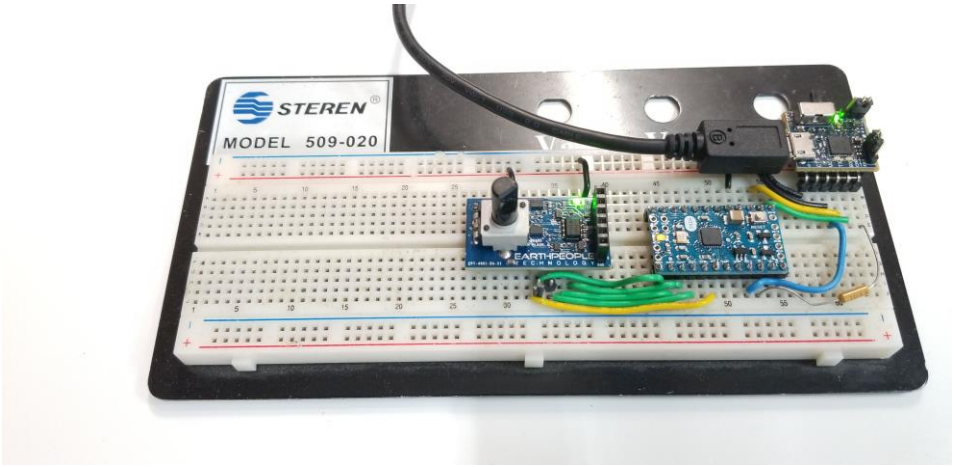
The write command is initiated by driving the CS pin low, followed by clocking the four Configuration bits and the 12 data bits into the SDI pin on the rising edge of SCK. The CS pin is then raised, causing the data to be latched into the DAC's input register. The MCP4901/4911/4921 utilizes a double-buffered latch structure to allow the analog output to be synchronized with the LDAC pin, if desired. By bringing the LDAC pin down to a low state, the content stored in the DAC's input register is transferred into the DAC's output register (VOUT), and VOUT is updated. All writes to the MCP4901/4911/4921 devices are 16-bit words. Any clocks past the 16th clock will be ignored. The Most Significant 4 bits are Configuration bits. The remaining 12 bits are data bits. No data can be transferred into the device with CS high. This transfer will only occur if 16 clocks have been transferred into the device. If the rising edge of CS occurs prior to that, shifting of data into the input register will be aborted.



3 Breadboard stackable headers



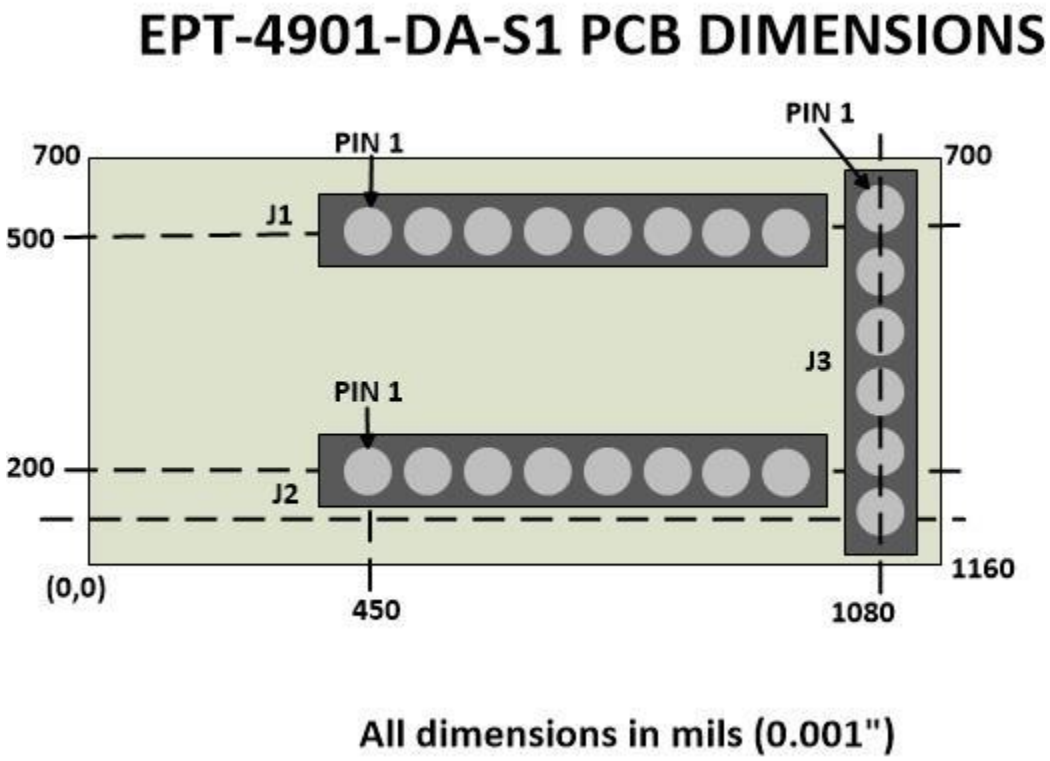
The breadboard headers of the EPT-4901-DA-S1 are surface mounted on the bottom of the board. The board mates perfectly with standard bread boards. The bread board connectors provide the access to the SPI bus. The DAC Vout is also available on the bread board connectors



3.1.1 Power Indication LED

The power LED sources current from the on board +3.3V power rail. When the EPT-4901-DA-S1 board is powered up by an external source either +3.3V or 5V, the LED will light up.

4 Mechanical Dimensions



5 Pin Mapping

EPT-4901-DA-S1 Pin Mapping

EPT-4901-DA-S1 Description	**EPT-4901-DA-S1 Connector Pin Number**	**EPT-4901-DA-S1 Connector**
VCC	1	J1
VCC	2	
NC	3	
NC	4	
NC	5	
NC	6	
GND	7	
GND	8	
VCC	1	J3
DAC_VOUT	2	
DAC_REF	3	
NC	4	
1NC	5	
GND	6	
DAC_VOUT	1	J2
FLASH_CS	2	
DAC_CS	3	

DAC_SCLK	4	
DAC_SDI	5	
FLASH_SDO	6	
DAC_LDAC	7	
GND	8	

6 Inputs/Outputs

The EPT-4901-DA-S1 I/O pins are compatible with either +3.3V or +5V. The EPT-4901-DA-S1 is powered from the +3.3V on pins 1 and 2 of J1. The board can be powered by either +3.3V and +5V. The digital inputs of the board should use the TTL values powered from the same source. as VCC.