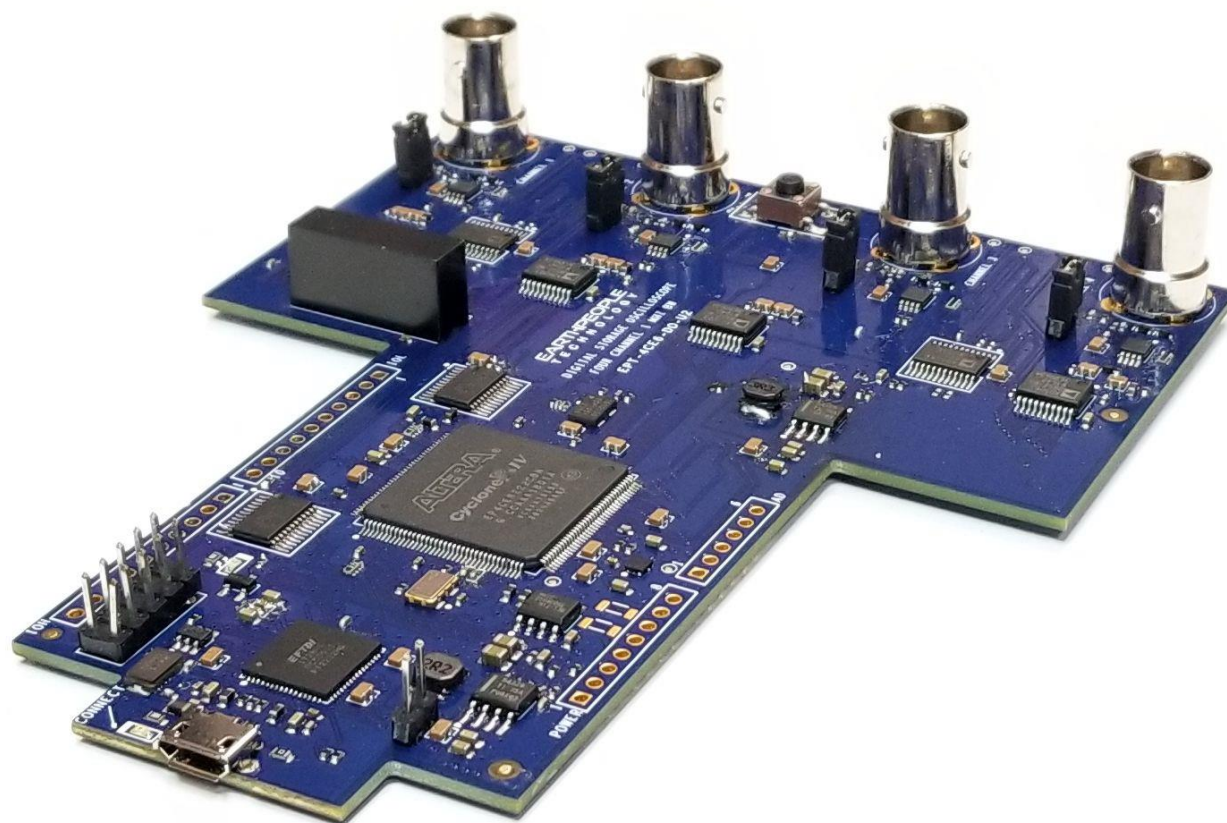


# DSO 100M DIGITAL STORAGE OSCILLOSCOPE DEVELOPMENT SYSTEM

## Data Sheet



The DSO 100M (EPT-4CE6-DO-U2) is a complete Digital Storage Oscilloscope development system. It provides four channels of analog input and four 80MHz ADC chips. The board connects to a USB Port on a Host PC. And, accepts commands and transfers data to the Host PC

The DSO 100M board is equipped with an Altera EP4CE6E22 FPGA; which is programmed using the Altera Quartus Prime software. The FPGA has 6,272 Logic Elements along with 276Kbits of RAM. An on board 66 MHz oscillator is used by the EPT-Active-Transfer-Library to provide data transfer rates of 8 Mega Bytes per second. The EPT-Active-Transfer-Library



## Data Sheet DSO Development System

provides control communication between the objective device and the FPGA. Data transfer during the objective device checkout between the PC and the FPGA program is available via the ActiveHost. The board also includes the following parts.

- Altera EP4CE6E22 FPGA in the TQFP 144 pin package
- 66 MHz oscillator for driving USB data transfers and users code
- 100 MHz oscillator for user clocking
- 63 user Input/Outputs
- 36 Green LED's accessible by the user
- Two PCB switches accessible by the user
- All connectors to stack into the Arduino DPL
- FPGA Configuration using the FT2232H Chip.
- Bi-Directional High Speed Data Transfer over USB.

## 1 Block Diagram

Figure 1 EPT-4CE6-DO-U2 Component Location

Data Sheet DSO Development System

**DSO 100M COMPONENT LOCATIONS**

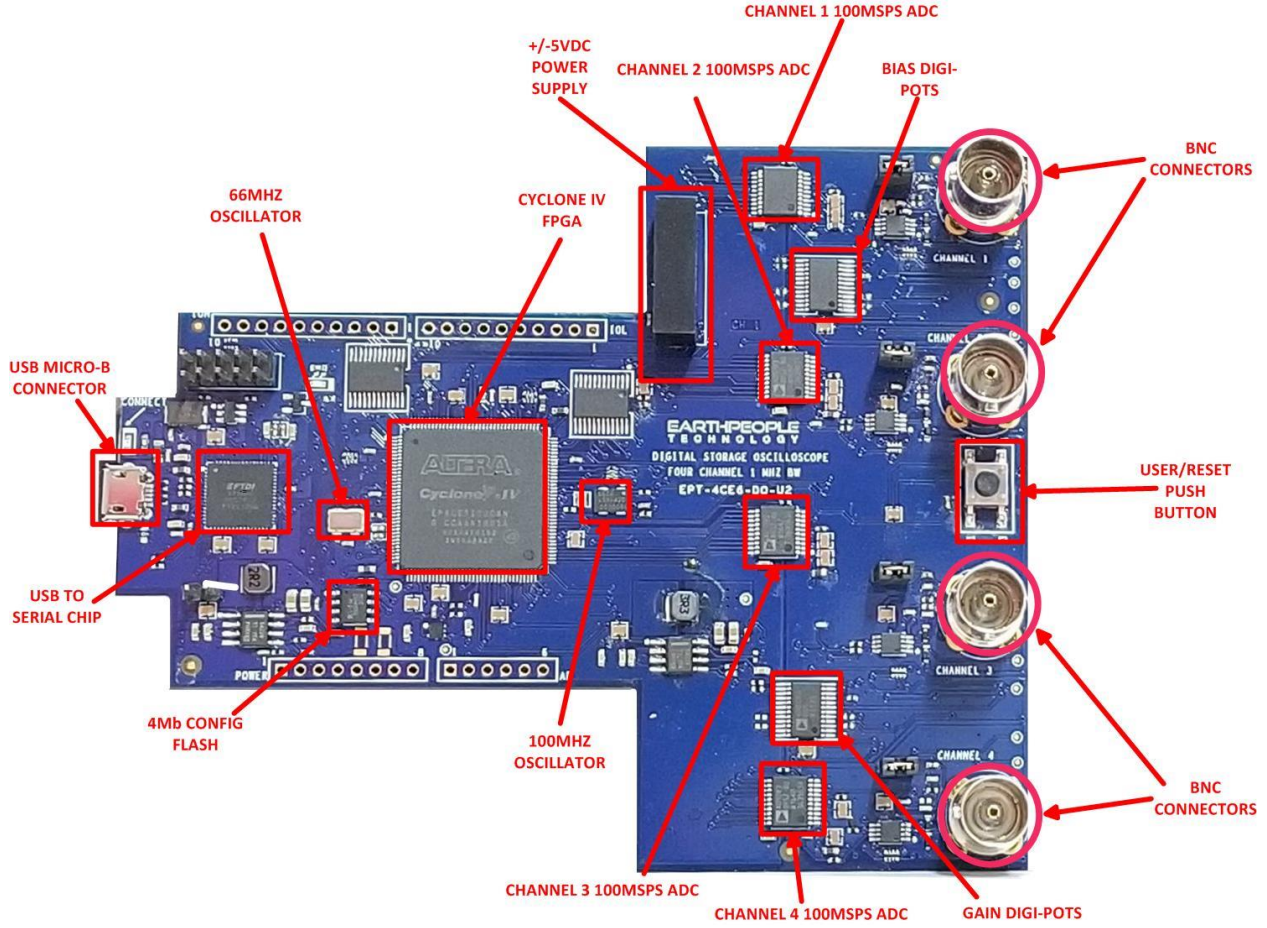
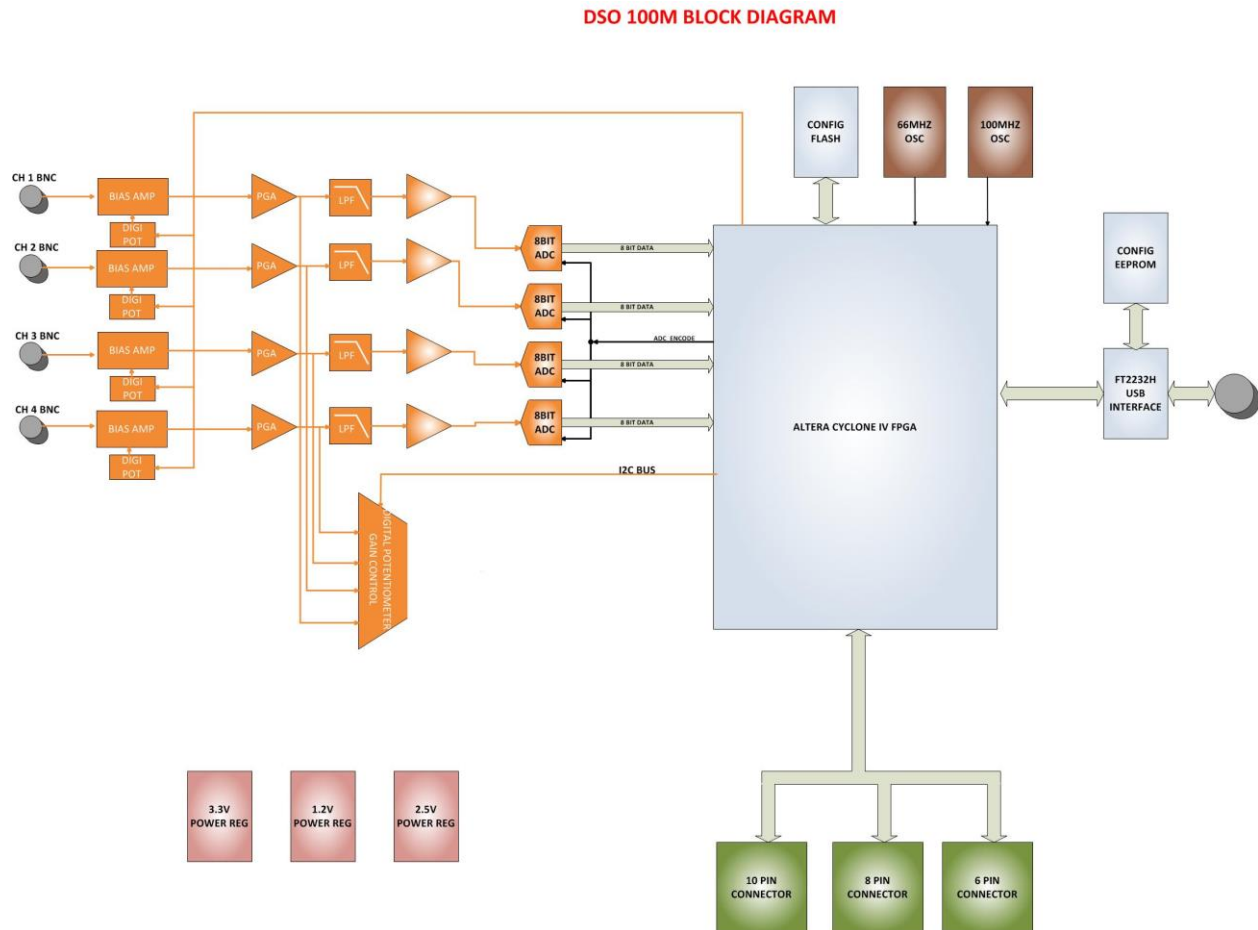


Figure 2 EPT-4CE6-DO-U2 Block Diagram



The user's microcontroller code is developed to perform particular functions required by the user. The code is downloaded to the device using the hardware/software system provided as part of the microcontroller development system. The DSO 100M Development System consists of an Intel FPGA, USB to Serial chip, Configuration flash, two separate oscillators, and two Bus Transceivers. The board has 63 User Input/Outputs available at 6 headers that match the Arduino Due board configuration. The board is powered by the USB Micro-B connector.

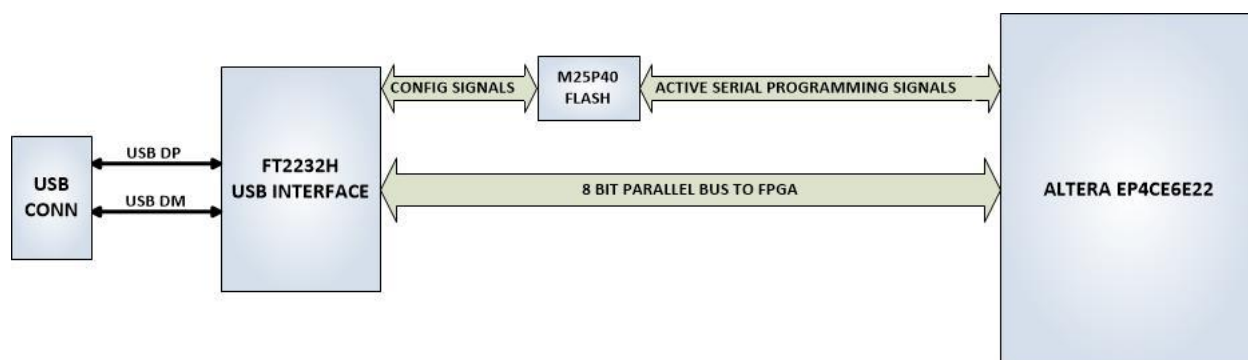
## 2 Mechanical Dimensions

## 3 Pin Mapping

## 4 Inputs/Outputs

## 5 FPGA Configuration

The EPT Blaster Driver will allow the Quartus Prime Software to program the Configuration Flash chip on the DSO 100M. The software will only access the M25P40 Flash chip. This chip is accessed from the FT2232H USB chip. Quartus will store the compiled and synthesized user code. After programming is complete, the FPGA automatically resets and reads the code from the Flash chip and programs itself using the Active Serial method.



## 6 Oscillators

TBD

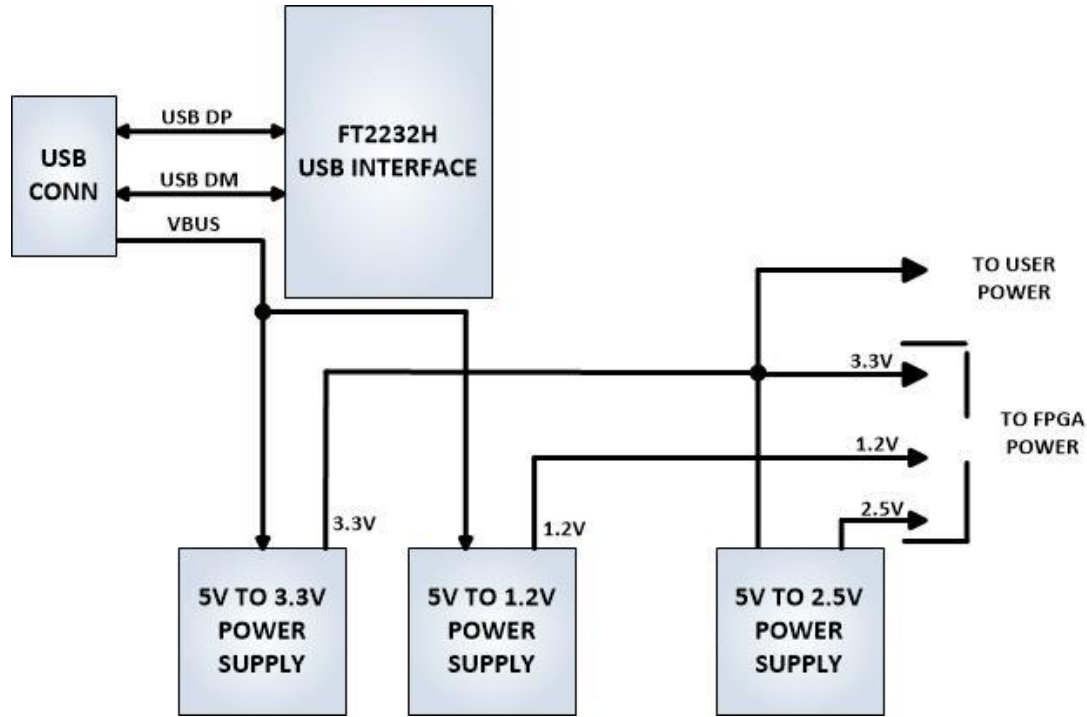
## 7 USB to Serial

TBD

## 8 DSO 100M Power

The DSO 100M can be powered from the USB bus of a Host/PC or the optional barrel connector. The USB supplies a maximum of +5V @ 500mA's. The components of the DSO 100M must share this power

with the user code that will run inside the FPGA along with any external power use.



### 8.1 Core Board Power Budget

Device	Part Number	+1.2V Power	+2.5V Power	+3.3V Power
FPGA	EP4CE6E22	50mA	10mA	50mA
Flash	M25P40			15mA (During the Write Status, Sector Erase, and Bulk Erase cycles)
USB Chip	FT2232H			60 mA (no sink current supplied to I/O's)
USB EEPROM	93LC56			2 mA (write current) 1 mA (read current)



## Data Sheet DSO Development System

66MHz Oscillator	FXO-HC536R-66			47 mA
100MHz Oscillator	FXO-HC536R-100			47 mA
Bus Transceivers	74LVC8T245PW,118			XXmA
Digital Pots	AD5263BRUZ50			XXmA
OPAMP AUDIO 35MHZ	OPA1602AIDGKR			XXmA
ADC 8BIT 80MSPS	AD9283BRSZ-RL80			XXmA
<b>Total</b>		<b>50mA</b>	<b>10mA</b>	<b>261mA</b>

\*Theoretical Values only. This data needs to be validated

## 8.2 Core Board VUSB Power Budget

Device	Part Number	VUSB		
+1.2V Power Supply	ISL9205IRZ	70mA		
+2.5V Power Supply	NCP360MU	12mA		
+3.3V Power Supply	LTC2952	275mA		
<b>Total</b>		<b>357mA</b>		

\* Theoretical Values only. This data needs to be validated