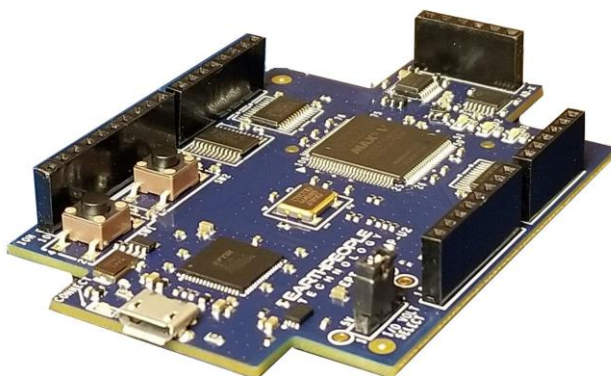


UnoMax CPLD Development System

Data Sheet



The UnoMax is a small form factor CPLD Development System. The core functions of the UnoMax are a two channel USB to Serial chip, 570 Logic Cell CPLD and a four channel 300KSample/Sec ADC. The board is powered from a USB port. The Input/Output connectors are organized to match the Arduino Uno. There is also an additional six pin header for the analog input signals.

The UnoMax is designed from the ground up as a development board for beginners. All of the Inputs/Outputs are protected by the 74LVC8245 transceiver chips. These transceivers provide both voltage level translations and protection from over current and over voltage. The transceivers can sink up to 50mA per pin. So, the UnoMax can drive LEDs and sensors directly. The analog inputs have a buffer amp on each input pin. Each Op-Amp on the analog inputs has a 1MHz filter

The board also includes the following parts.

- Intel/Altera 5M570 CPLD with 440 Macrocells
- 4 Channel ADC 300KSamples/Second
- 66 MHz oscillator for driving USB data transfers and users code
- Three bidirectional voltage translator/bus transceivers
- 24 user Input/Outputs available as three 8 bit ports
- Ports have jumper selectable 3.3V/5 Volt Input/Output
- Four Green LED's accessible by the user
- Two PCB switches accessible by the user

1 Block Diagram

Figure 1-1 UnoMax Component Location

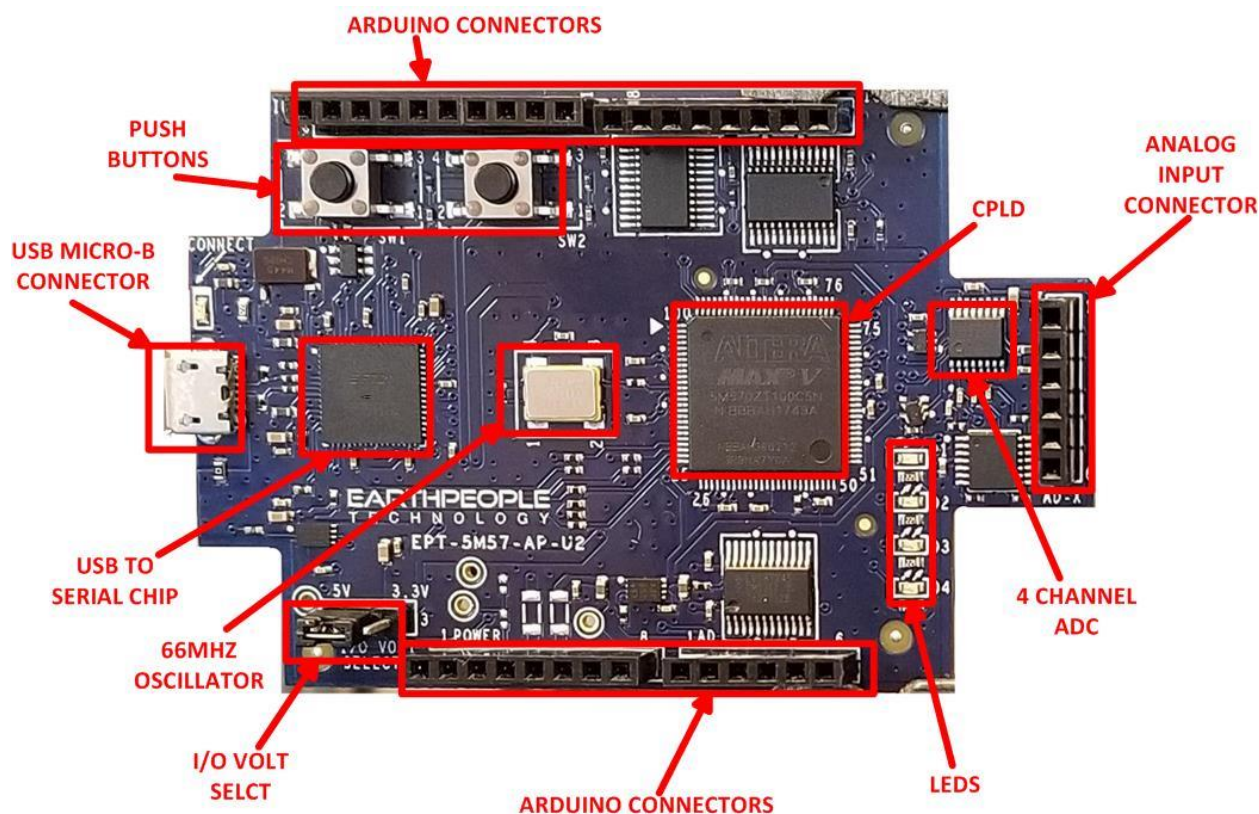
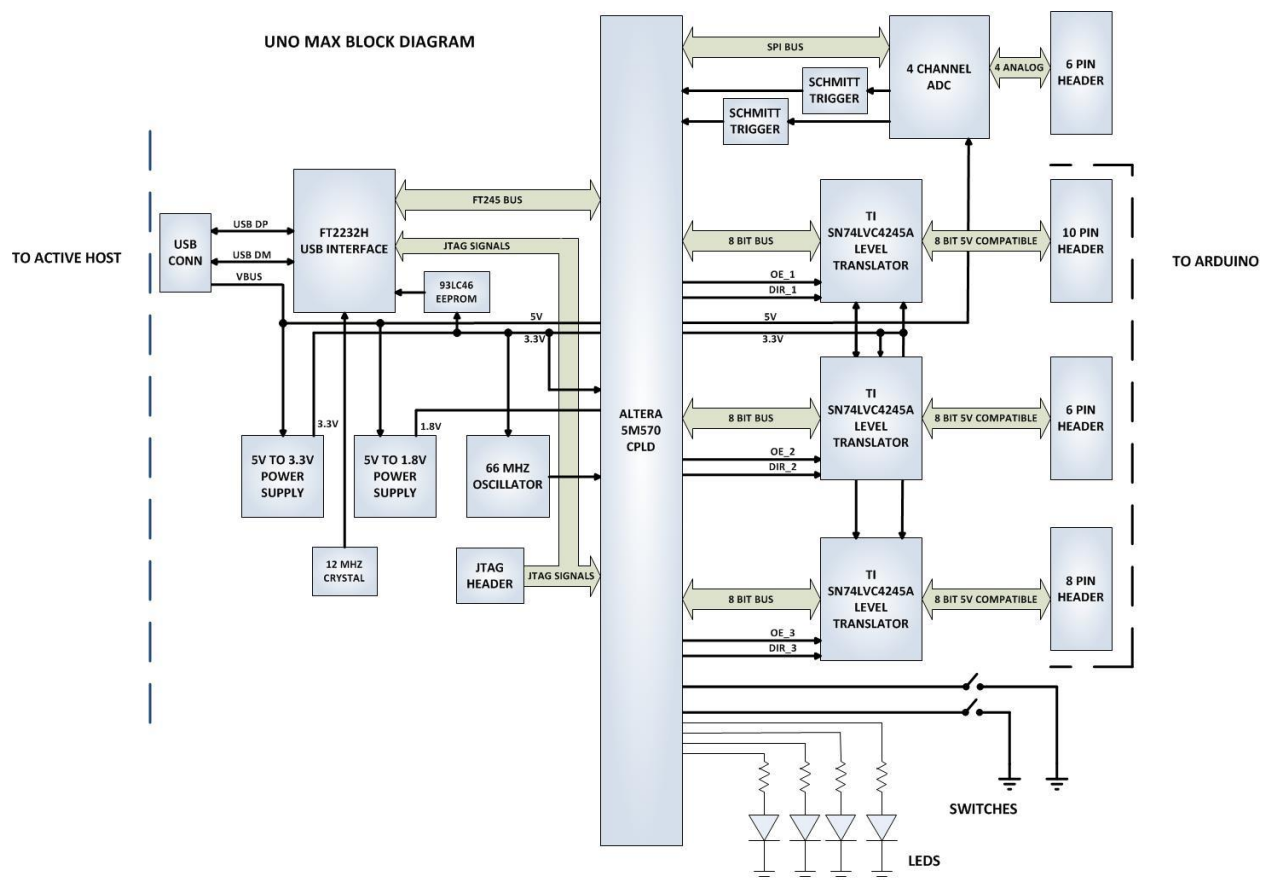
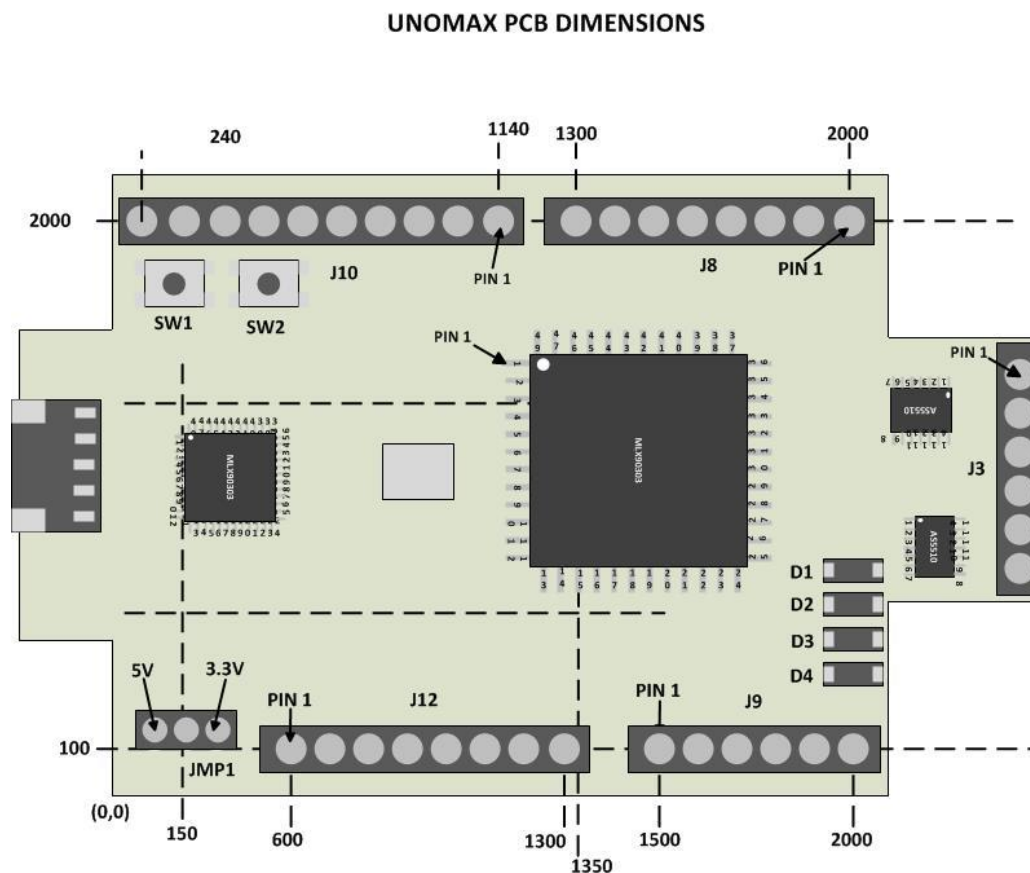


Figure 1-2 UnoMax Block Diagram



2 Mechanical Dimensions

Figure 2-1 UnoMax Mechanical Dimensions



All dimensions in mils (0.001")

3 Pin Mapping

Figure 3-1. Pin Mapping between Connectors, MAXV CPLD and User code

| Component | Pin | Net Name | Pin on CPLD | Signal in EPT Project Pinout |
|------------------|-----|----------|-------------|------------------------------|
| 66MHz Oscillator | 3 | GCLK | 12 | aa[1] |

CPLD Development System Data Sheet

| | | | | |
|-------|----|-----------|-----|---------------------------|
| Reset | 2 | NA | 44 | aa[0] |
| U12 | 16 | AD0 | 24 | JTAG_TCK (Not In Project) |
| | 17 | AD1 | 23 | JTAG_TDI (Not In Project) |
| | 18 | AD2 | 25 | JTAG_TDO (Not In Project) |
| | 19 | AD3 | 22 | JTAG_TMS (Not In Project) |
| | 38 | BD0 | 19 | BD_INOUT0 |
| | 39 | BD1 | 18 | BD_INOUT1 |
| | 40 | BD2 | 17 | BD_INOUT2 |
| | 41 | BD3 | 16 | BD_INOUT3 |
| | 43 | BD4 | 15 | BD_INOUT4 |
| | 44 | BD5 | 14 | BD_INOUT5 |
| | 45 | BD6 | 7 | BD_INOUT6 |
| | 46 | BD7 | 6 | BD_INOUT7 |
| | 48 | BC0 | 5 | BC_IN1 |
| | 52 | BC1 | 4 | BC_IN0 |
| | 53 | BC2 | 3 | BC_OUT2 |
| | 54 | BC3 | 2 | BC_OUT1 |
| | 55 | BC4 | 1 | BC_OUT0 |
| SW1 | 1 | SW_USER_1 | 20 | SW_USER_1 |
| SW2 | 1 | SW_USER_2 | 21 | SW_USER_23 |
| U7 | 2 | TR_DIR_1 | 100 | TR_DIR_1 |

CPLD Development System Data Sheet

| | | | | |
|----|----|------------|----|-----------|
| U4 | 2 | TR_DIR_2 | 29 | TR_DIR_2 |
| U5 | 2 | TR_DIR_3 | 85 | TR_DIR_3 |
| U7 | 22 | TR_OE_1 | 86 | TR_OE_1 |
| U4 | 22 | TR_OE_2 | 28 | TR_OE_2 |
| U5 | 22 | TR_OE_3 | 74 | TR_OE_3 |
| D1 | 1 | LED_GR_1_N | 54 | LED0 |
| D2 | 1 | LED_GR_2_N | 53 | LED1 |
| D3 | 1 | LED_GR_3_N | 52 | LED2 |
| D4 | 1 | LED_GR_4_N | 51 | LED3 |
| U9 | 16 | ADC_EOC | 67 | ADC_EOC |
| | 12 | ADC_CS | 68 | ADC_CS |
| | 13 | ADC_SCLK | 69 | ADC_CLK |
| | 14 | ADC_DIN | 70 | ADC_MOSI |
| | 15 | ADC_DOUT | 71 | ADC_MISO |
| | 8 | ADC_CNVST | 72 | ADC_CNVST |
| U7 | 21 | LB0 | 87 | LB_IOH0 |
| | 20 | LB1 | 89 | LB_IOH1 |
| | 19 | LB2 | 91 | LB_IOH2 |
| | 18 | LB3 | 92 | LB_IOH3 |
| | 17 | LB4 | 96 | LB_IOH4 |
| | 16 | LB5 | 97 | LB_IOH5 |
| | 15 | LB6 | 98 | LB_IOH6 |
| | 14 | LB7 | 99 | LB_IOH7 |

CPLD Development System Data Sheet

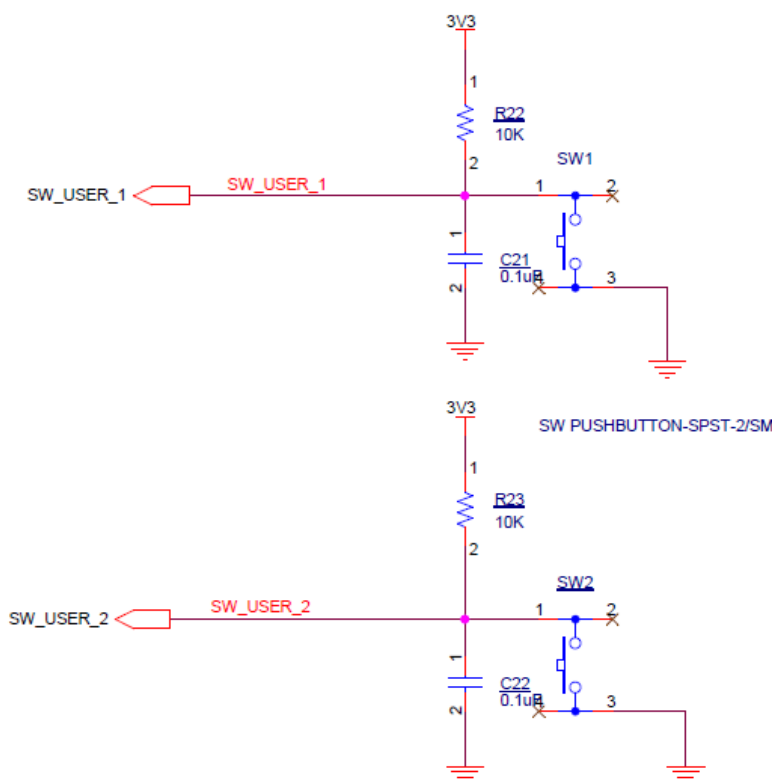
| | | | | |
|----|----|------|----|---------|
| U4 | 21 | LB8 | 42 | LB_SER0 |
| | 20 | LB9 | 41 | LB_AD0 |
| | 19 | LB10 | 40 | LB_AD1 |
| | 18 | LB11 | 38 | LB_AD2 |
| | 17 | LB12 | 36 | LB_AD3 |
| | 16 | LB13 | 35 | LB_AD4 |
| | 15 | LB14 | 34 | LB_AD5 |
| | 14 | LB15 | 33 | LB_SER1 |
| U5 | 21 | LB16 | 81 | LB_IOL0 |
| | 20 | LB17 | 82 | LB_IOL1 |
| | 19 | LB18 | 83 | LB_IOL2 |
| | 18 | LB19 | 84 | LB_IOL3 |
| | 17 | LB20 | 78 | LB_IOL4 |
| | 16 | LB21 | 77 | LB_IOL5 |
| | 15 | LB22 | 76 | LB_IOL6 |
| | 14 | LB23 | 75 | LB_IOL7 |

4 Pushbutton switches

The UnoMax includes two push button switches. Both are momentary contact switches. They include a 1uF cap to ground to debounce both switches.

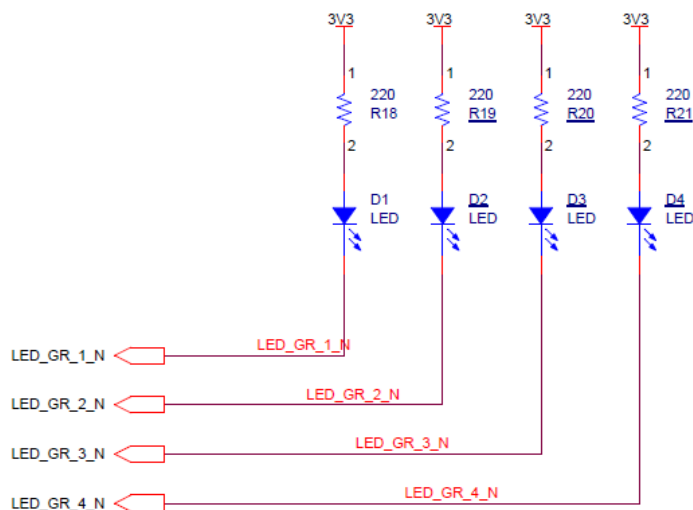
| Component | Net Name | Pin on CPLD | Signal in EPT Project Pinout |
|-----------|----------|-------------|------------------------------|
| | | | |

| | | | |
|-----|-----------|----|------------|
| SW1 | SW_USER_1 | 20 | SW_USER_1 |
| SW2 | SW_USER_2 | 21 | SW_USER_23 |



5 LEDs

The UnoMax includes four Green LEDs. The LEDs are connected to the CPLD in a “Current Sink” configuration. This means the LEDs Anodes are permanently connected to +3.3V. Each Cathode side of the LEDs are connected to an individual I/O of the CPLD. In order to turn on the LED, the CPLD I/O must apply a low signal. This will complete the LED drive circuit and current will flow through the LED. To turn the LED off, the CPLD I/O must either “float” or drive a high onto the pin.



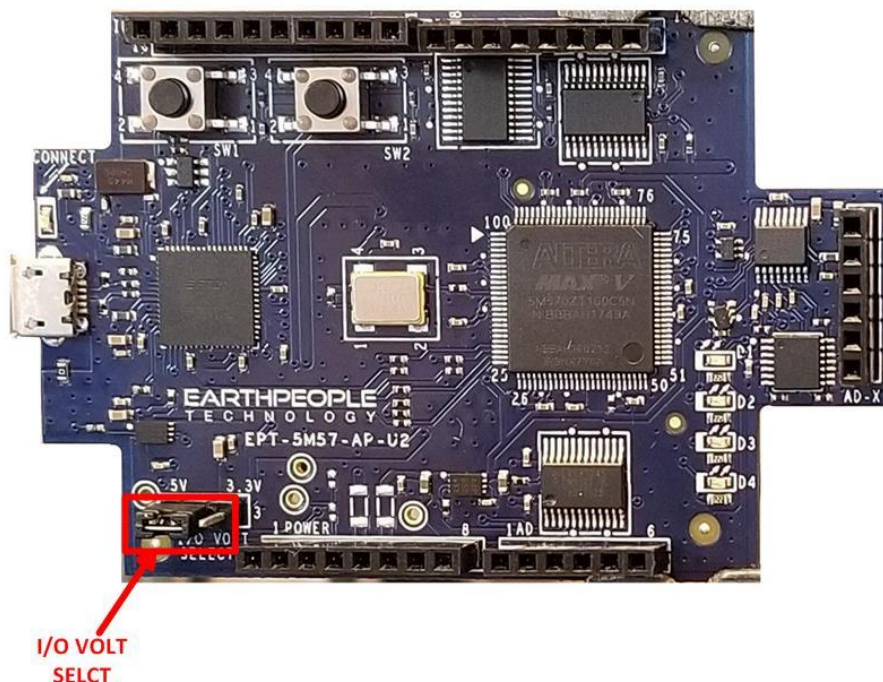
| Component | Net Name | Pin on FPGA | Signal in EPT Project Pinout |
|-----------|----------|-------------|------------------------------|
| LED1 | LED[1] | 50 | LED[0] |
| LED2 | LED[2] | 51 | LED[1] |
| LED3 | LED[3] | 52 | LED[2] |
| LED4 | LED[4] | 53 | LED[3] |

6 Inputs/Outputs

The UnoMax is designed from the ground up as a development board for beginners. All of the Inputs/Outputs are protected by the 74LVC8245 transceiver chips. These transceivers provide both voltage level translations and protection from over current and over voltage. The transceivers can sink up to 50mA per pin.

There are 24 Inputs/Outputs which are selectable between +3.3V and +5 Volt. JMP1 is used to

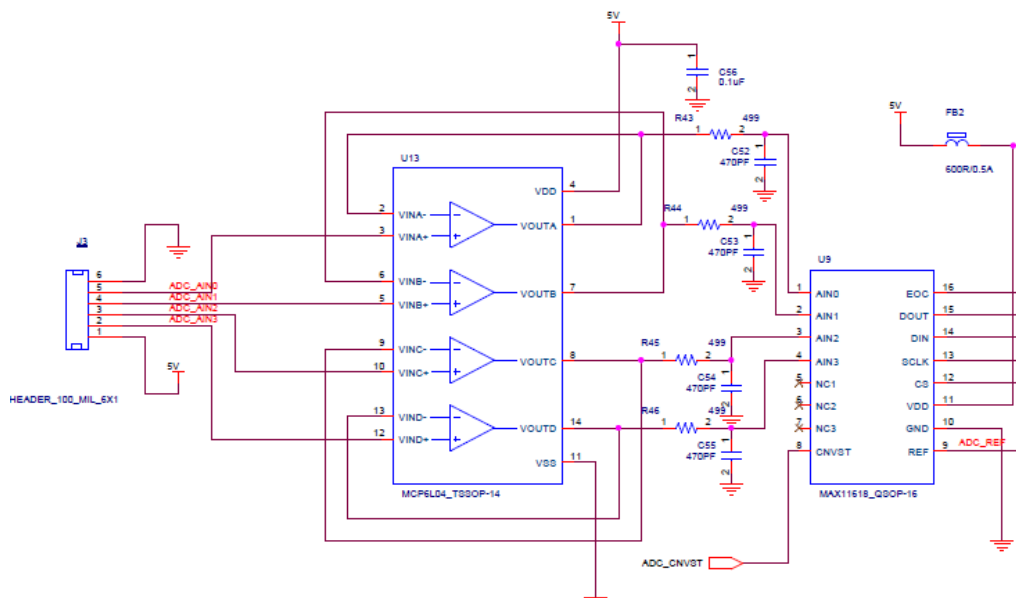
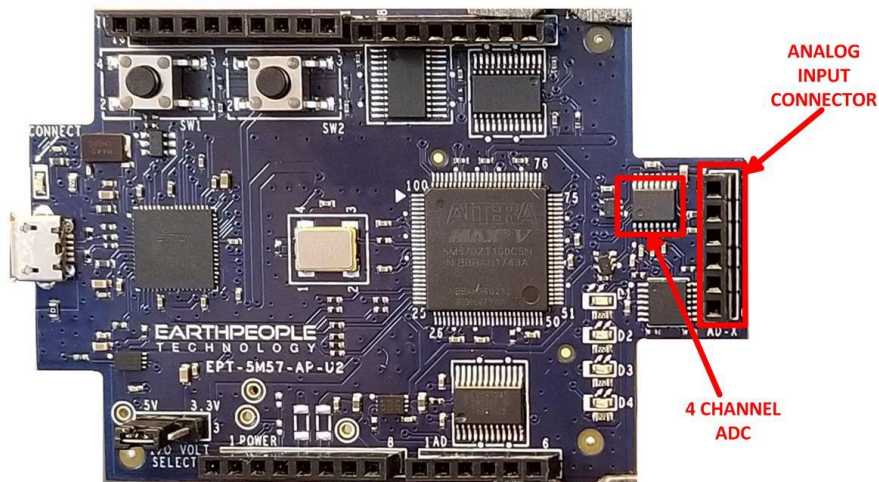
select which voltage the 24 Inputs/Outputs are set to.



The I/O's are organized as three 8 bit directional ports. Each port must be defined as input or output. This means that all 8 bits of a port will point in the same direction, depending on the direction bit of the transceiver. The direction bit can be changed at any time, so that a port can change from input to output in minimum setup time of 6 nanoseconds. Each port also has an enable pin. This enable pin will enable or disable the bits of the port. If the port is disabled, the bits will “float”.

7 Analog connector

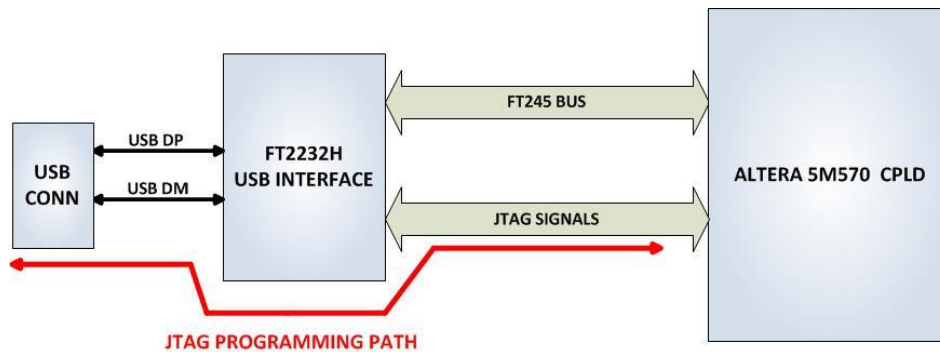
The UnoMax includes a six pin analog input connector. This connector provides a path from the pins to the input of the four Op-Amp buffers. Each Op-Amp includes a 1MHz low pass filter. Each Op-Amp provides a buffer for the analog signals to the ADC inputs.



8 MAXV Programming

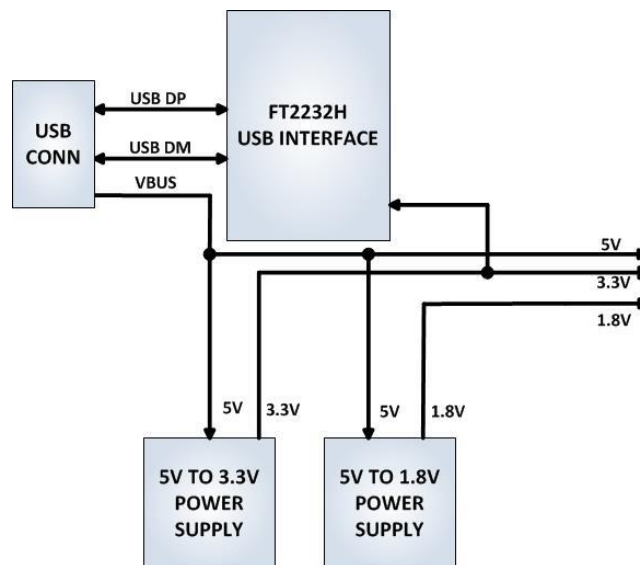
The UnoMax uses the second channel of the FT2232H chip as a dedicated CPLD programming port. The CPLD must be programmed via JTAG signals and the FT2232H has built in JTAG

signals.



9 UnoMax Power

The UnoMax is powered from the USB bus of a Host/PC. The USB supplies a maximum of +5V @ 500mA's. The components of the UnoMax must share this power with the user code that will run inside the CPLD along with any external power use.



1.1.1 Core Board Power Budget

| Device | Part Number | +1.8V Power | +3.3V Power |
|--------|-------------|-------------|-------------|
|--------|-------------|-------------|-------------|

CPLD Development System Data Sheet

| | | | |
|------------------|---------------|--|--|
| CPLD | 5M570 | ??? Defined by user code. EPT-Transfer-Demo code: 50mA | ??? Defined by user code. . EPT-Transfer-Demo code: 50mA |
| Bus Transceivers | 74LVC8245 | | 15mA (All eight I/O's active) |
| USB Chip | FT2232H | | 60 mA (no sink current supplied to I/O's) |
| USB EEPROM | 93LC56 | | 2 mA (write current) 1 mA (read current) |
| 66MHz Oscillator | CB3LV-3I-66M0 | | 10 mA |
| ADC Four Channel | MAX11618EEE+ | | 17 mA |
| Op-Amp driver | MCP6L04 | | 0.5 mA (all four amps active) |
| Schmitt Buffer | 74LVC1G17SE | | 1mA |
| User LEDs | | | 20 mA |
| Total | | 50mA | 175.5mA |

*Theoretical Values only. This data needs to be validated

1.1.2 Core Board VUSB Power Budget

| Device | Part Number | VUSB | | |
|--------------------|--------------------|--------------|--|--|
| +1.8V Power Supply | MCP1725-1802E | 70mA | | |
| +3.3V Power Supply | MCP1725-3302E | 215mA | | |
| Total | | 285mA | | |

* Theoretical Values only. This data needs to be validated