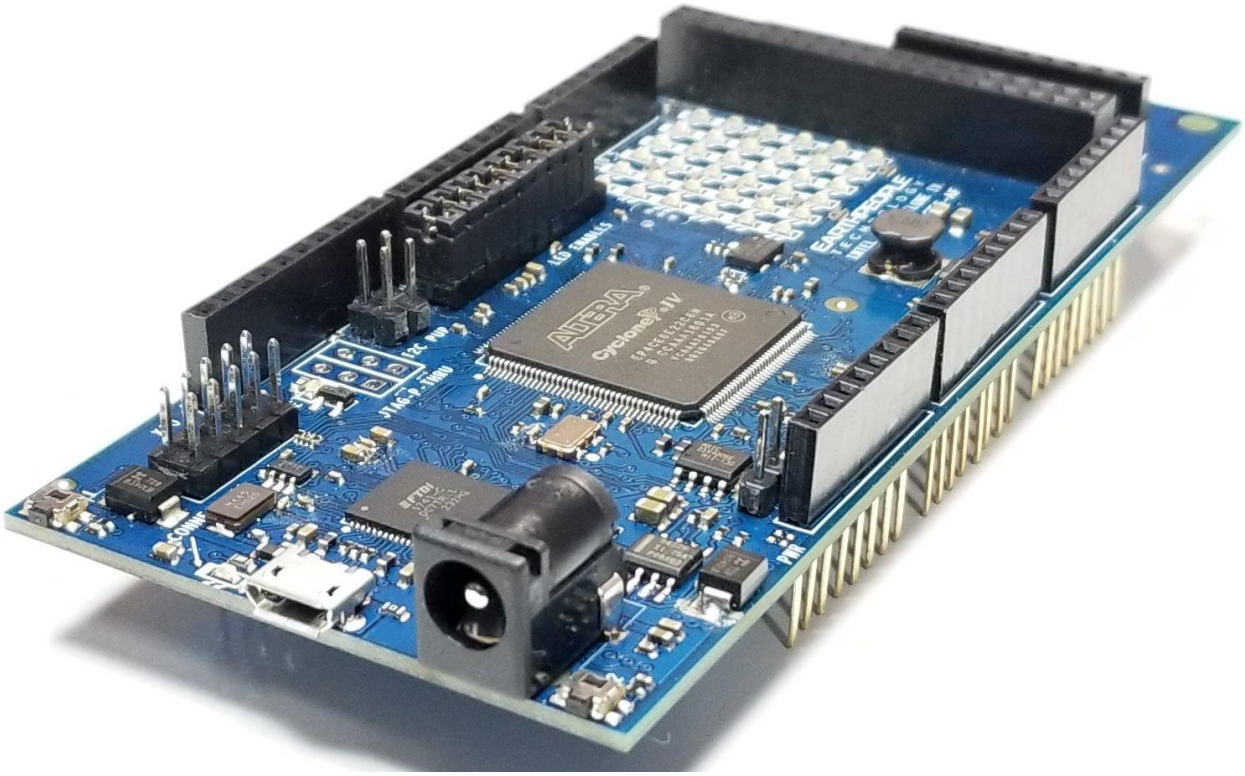
DUEPROLOGIC

FPGA DEVELOPMENT SYSTEM

Data Sheet



The DueProLogic (EPT-4CE6-AF-D2) is a part of the EPT USB/FPGA development system. It provides an innovative method of developing and debugging the users microcontroller code. It can also provide a high speed data transfer mechanism between microcontroller and Host PC.

The EPT-4CE6-AF-D2 board is equipped with an Altera EP4CE6E22 FPGA; which is programmed using the Altera Quartus Prime software. The FPGA has 6,272 Logic Elements

along with 276Kbits of RAM. An on board 66 MHz oscillator is used by the EPT-Active-Transfer-Library to provide data transfer rates of 8 Mega Bytes per second. The EPT-Active-Transfer-Library provides control communication between the objective device and the FPGA. Data transfer during the objective device checkout between the PC and the FPGA program is available via the ActiveHost. The board also includes the following parts.

- Altera EP4CE6E22 FPGA in the TQFP 144 pin package
- 66 MHz oscillator for driving USB data transfers and users code
- 100 MHz oscillator for user clocking
- 63 user Input/Outputs
- 36 Green LED's accessible by the user
- Two PCB switches accessible by the user
- All connectors to stack into the Arduino from DPL
- FPGA Configuration using the FT2232H Chip.
- Bi-Directional High Speed Data Transfer over USB.

1 Block Diagram

Figure 1 EPT-4CE6-AF Component Location

Data Sheet EPT FPGA Development System

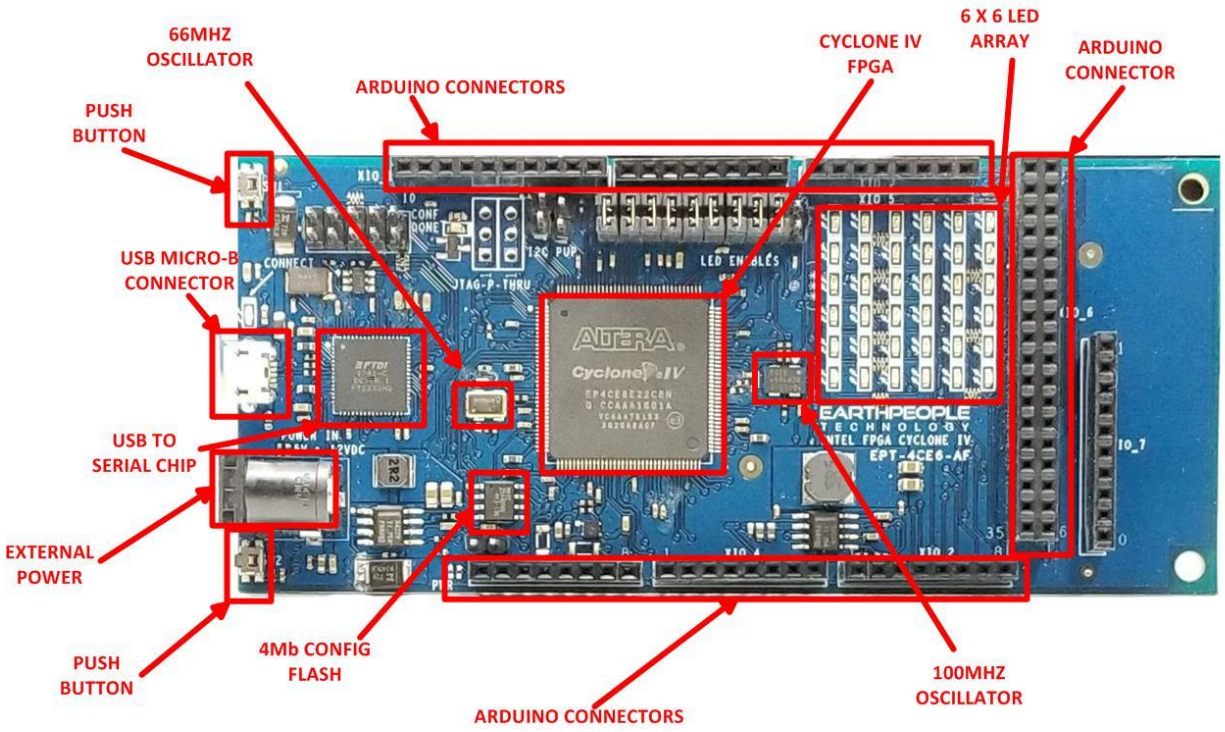
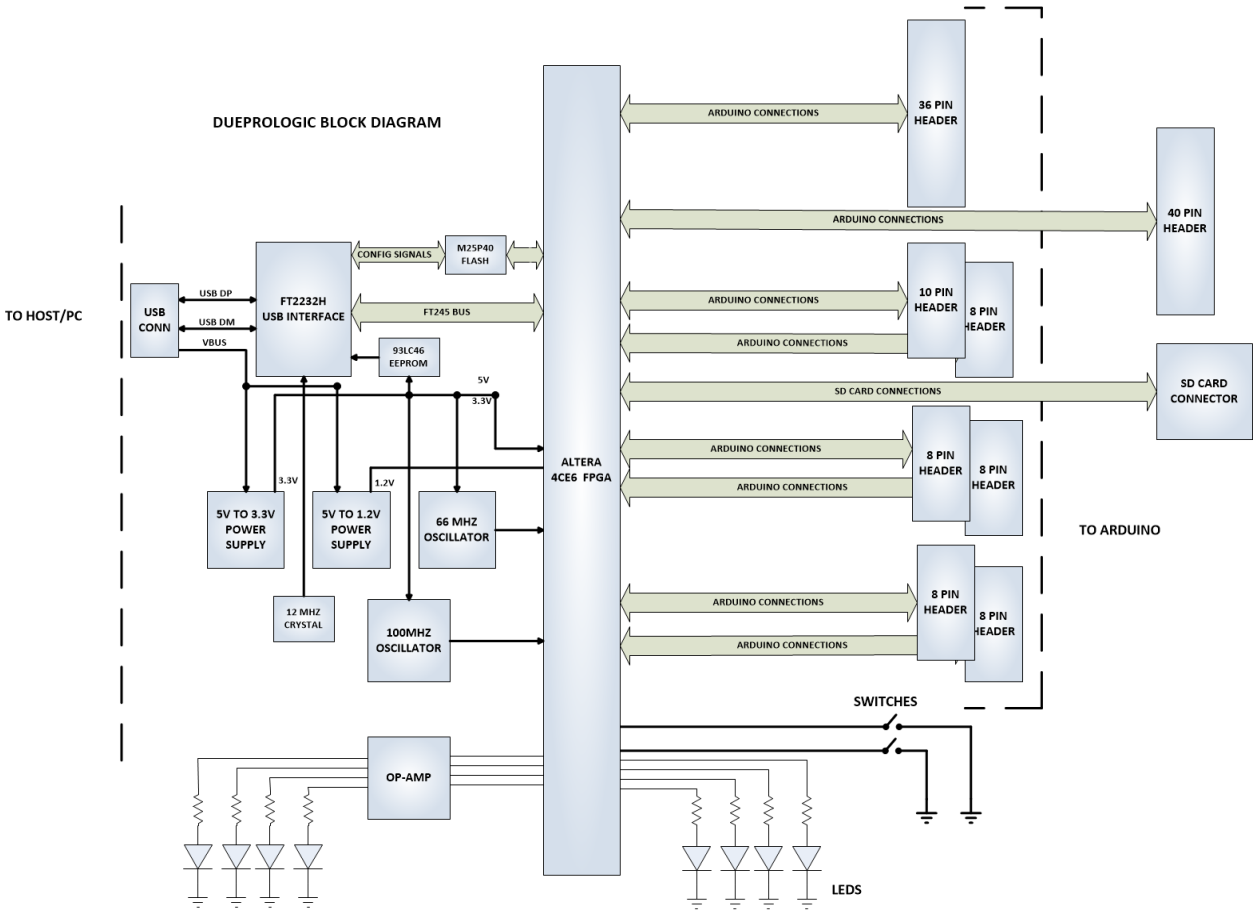


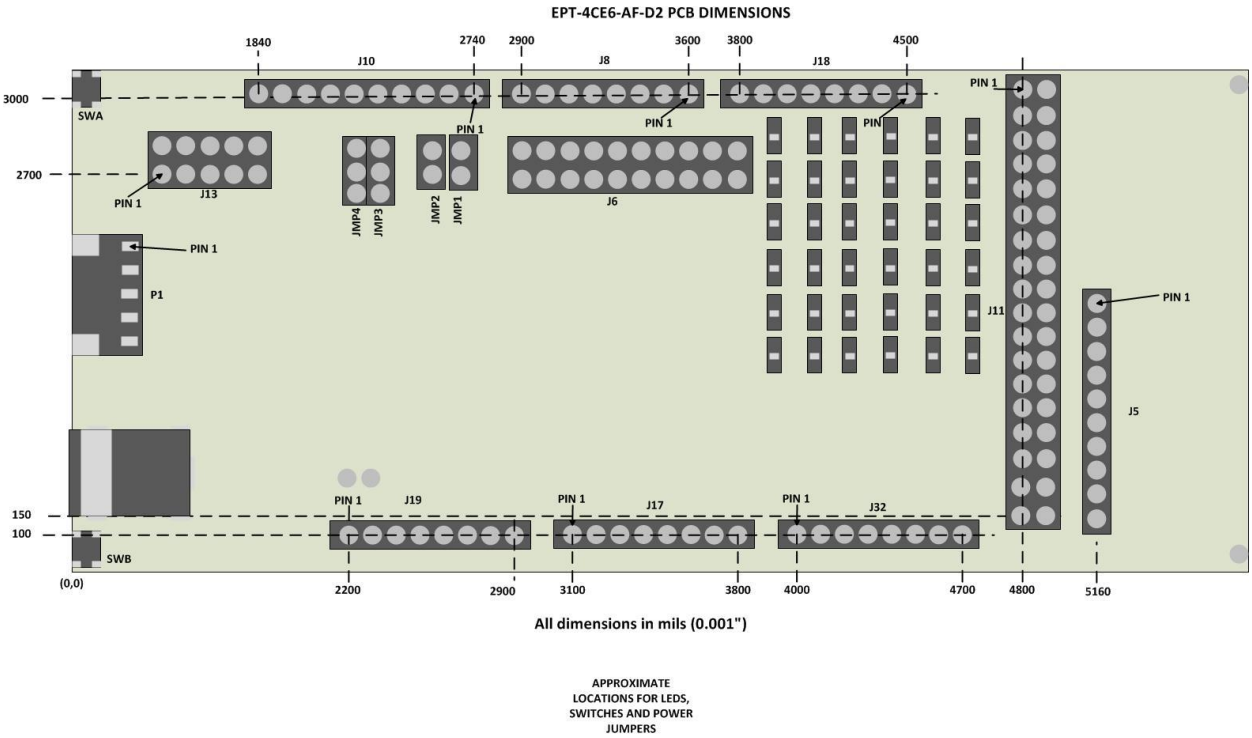
Figure 2 EPT-4CE6-AF Block Diagram



The user's microcontroller code is developed to perform particular functions required by the user. The code is downloaded to the device using the hardware/software system provided as part of the microcontroller development system. The DueProLogic USB/FPGA Development System consists of an Intel FPGA, USB to Serial chip, Configuration flash, two separate oscillators, SD Card slot, two push buttons and 36 LEDs. The board has 63 User Input/Outputs available at 6 headers that match the Arduino Due board configuration. There are two power options, USB Micro-B connector or Barrel Connector.

2 Mechanical Dimensions

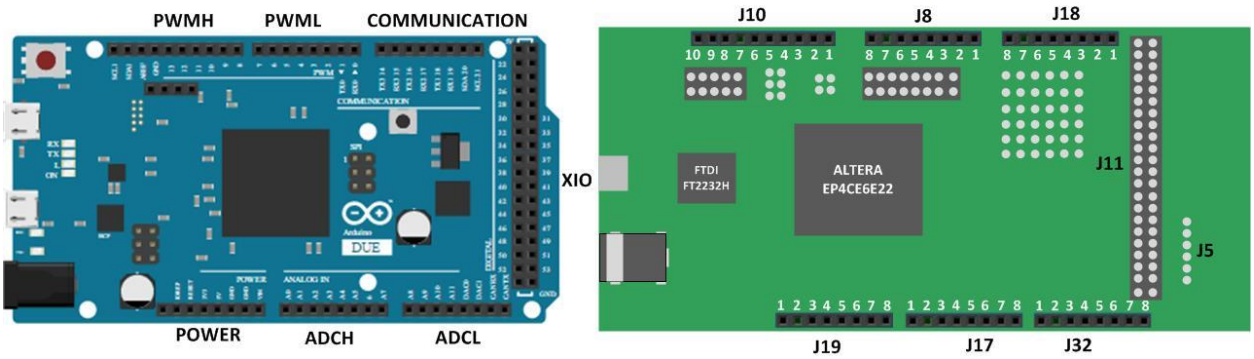
Figure 3 EPT-4CE6-AF Mechanical Dimensions



3 Pin Mapping

Figure 4. Pin Mapping between Arduino Due, DueProLogic and FPGA User code

DUE TO DUEPROLOGIC PIN MAPPING



Arduino Due Connector Pin	**DuePrologic Connector-Pin #**	**DuePrologic Net Name**	**DuePrologic FPGA Pin Number**	**DuePrologic FPGA User Code Signal Name**
	J10-1	UB0	136	XIO1[0]
	J10-2	UB1	137	XIO1[1]
	J10-3	UB2	138	XIO1[2]
	J10-4	UB3	141	XIO1[3]
	J10-5	UB4	142	XIO1[4]
	J10-6	UB5	143	XIO1[5]
	J10-7	GND	NC	NC
	J10-8	3V3	NC	NC
	J10-9	UB6	144	XIO1 [6]
	J10-10	UB7	7	XIO1[7]

Arduino Due Connector Pin	DuePrologic Connector-Pin #	DuePrologic Net Name	DuePrologic FPGA Pin Number	DuePrologic FPGA User Code Signal Name
	J32-1	3V3	NC	NC
	J32-2	UB9	52	XIO2[0]
	J32-3	UB10	53	XIO2[1]
	J32-4	UB11	66	XIO2[2]
	J32-5	UB12	67	XIO2[3]
	J32-6	UB13	54	XIO2[4]
	J32-7	UB14	55	XIO2[5]
	J32-8	GND	NC	NC

Arduino Due Connector Pin	DuePrologic Connector-Pin #	DuePrologic Net Name	DuePrologic FPGA Pin Number	DuePrologic FPGA User Code Signal Name
	J8-1	3V3	NC	NC
	J8-2	UB16	127	XIO3[0]
	J8-3	UB17	128	XIO3[1]
	J8-4	UB18	129	XIO3[2]
	J8-5	UB19	132	XIO3[3]
	J8-6	UB20	133	XIO3[4]
	J8-7	UB21	135	XIO3[5]

	J8-8	GND	NC	NC

Arduino Due Connector Pin	**DuePrologic Connector-Pin #**	**DuePrologic Net Name**	**DuePrologic FPGA Pin Number**	**DuePrologic FPGA User Code Signal Name**
	J17-1	VIN	NC	NC
	J17-2	UB65	31	XIO4[0]
	J17-3	UB64	46	XIO4[1]
	J17-4	UB63	44	XIO4[2]
	J17-5	UB62	42	XIO4[3]
	J17-6	UB61	49	XIO4[4]
	J17-7	UB60	50	XIO4[5]
	J17-8	GND	NC	NC

Arduino Due Connector Pin	**DuePrologic Connector-Pin #**	**DuePrologic Net Name**	**DuePrologic FPGA Pin Number**	**DuePrologic FPGA User Code Signal Name**
	J18-1	VIN	NC	NC
	J18-2	UB54	119	XIO5[0]
	J18-3	UB55	120	XIO5[1]
	J18-4	UB56	121	XIO5[2]
	J18-5	UB57	124	XIO5[3]

	J18-6	UB58	125	XIO5[4]
	J18-7	UB59	126	XIO5[5]
	J18-8	GND	NC	NC

Arduino Due Connector Pin	**DuePrologic Connector-Pin #**	**DuePrologic Net Name**	**DuePrologic FPGA Pin Number**	**DuePrologic FPGA User Code Signal Name**
	J11-1	3V3	NC	NC
	J11-2	VIN	NC	NC
	J11-3	UB22	115	XIO6[0]
	J11-4	UB23	114	XIO6[1]
	J11-5	UB24	113	XIO6[2]
	J11-6	UB25	112	XIO6[3]
	J11-7	UB26	111	XIO6[4]

	J11-8	UB27	110	XIO6[5]
	J11-9	UB28	106	XIO6[6]
	J11-10	UB29	105	XIO6[7]
	J11-11	UB23	104	XIO6[8]
	J11-12	UB31	103	XIO6[9]
	J11-13	UB32	101	XIO6[10]
	J11-14	UB33	100	XIO6[11]
	J11-15	UB34	99	XIO6[12]
	J11-16	UB35	98	XIO6[13]
	J11-17	UB36	58	XIO6[14]
	J11-18	UB37	51	XIO6[15]
	J11-19	UB38	65	XIO6[16]
	J11-20	UB39	87	XIO6[17]
	J11-21	UB40	86	XIO6[18]
	J11-22	UB41	85	XIO6[19]
	J11-23	UB42	84	XIO6[20]
	J11-24	UB43	83	XIO6[21]
	J11-25	UB44	80	XIO6[22]
	J11-26	UB45	77	XIO6[23]
	J11-27	UB46	76	XIO6[24]
	J11-28	UB47	73	XIO6[25]

	J11-29	UB48	74	XIO6[26]
	J11-30	UB49	75	XIO6[27]
	J11-31	UB50	72	XIO6[28]
	J11-32	UB51	71	XIO6[29]
	J11-33	UB52	70	XIO6[30]
	J11-34	UB53	69	XIO6[31]

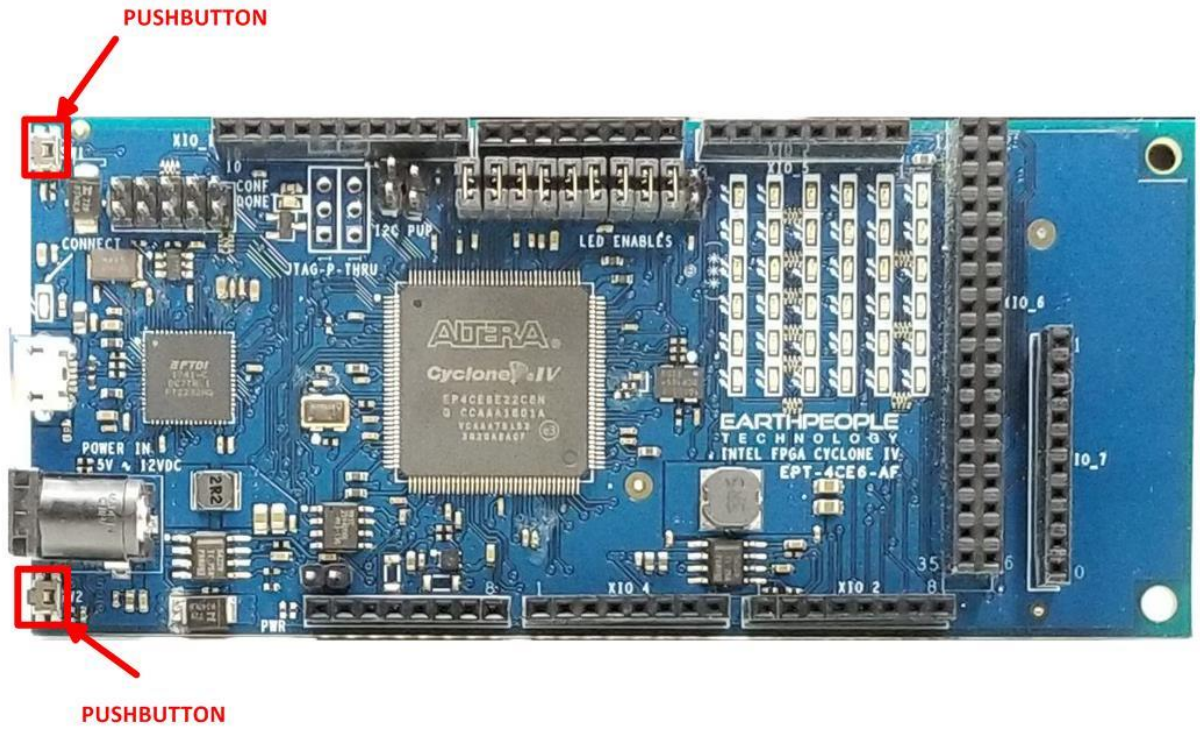
Arduino Due Connector Pin	**DuePrologic Connector-Pin #**	**DuePrologic Net Name**	**DuePrologic FPGA Pin Number**	**DuePrologic FPGA User Code Signal Name**
	J5-1	VIN	NC	NC
	J5-2	3V3	NC	NC
	J5-3	NC	NC	NC
	J5-4	NC	NC	NC
	J5-5	UB71	59	XIO7[3]
	J5-6	UB70	60	XIO7[2]
	J5-7	UB55	120	UART_TXD
	J5-8	UB54	119	UART_RXD
	J5-9	GND	NC	NC
	J5-10	GND	NC	NC

2	D62	SD_DATA[0]
1	D68	SD_DATA[1]

4 Pushbutton switches

There are two pushbutton switches on the DueProLogic. Both are momentary contact switches. They include a 1uF cap to ground to debounce both switches.

Component	**Net Name**	**Pin on FPGA**	**Signal in EPT Project Pinout**	
SW1	UB66	25	UBA	
SW2	UB67	24	UBB	



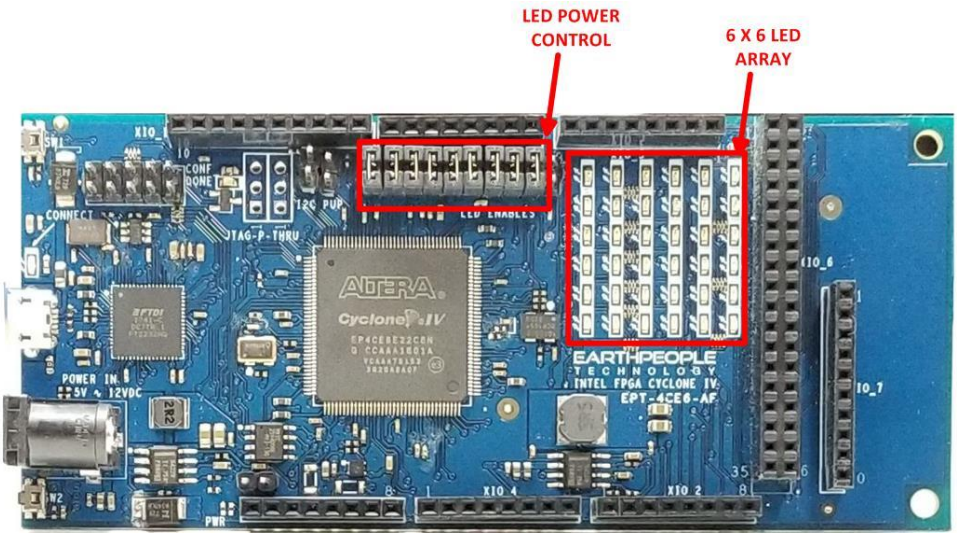
5 LEDs

There are 38 total LEDs on the DueProLogic. One Green LED to denote when the Windows PC has discovered and enumerated the DueProLogic. One Green LED to denote when the Cyclone IV FPGA has been configured properly. And 36 Green LEDs for user programming. The 36 Green User LEDs are sinked directly from the Cyclone IV FPGA. Each LED uses a 220 Ohm resistor connected to +3.3V. The LED is driven with 5.4 mA's of current. There is also a jumper selectable power enable for each four block group of LEDs. This allows the user to turn off the LEDs and use the FPGA pin as Input/Output on the 36 pin connector.

Component	**Net Name**	**Pin on FPGA**	**Signal in EPT Project Pinout**
LED0	UB22	TBD	XIO_6 [0]
LED1	UB23	TBD	XIO_6 [1]

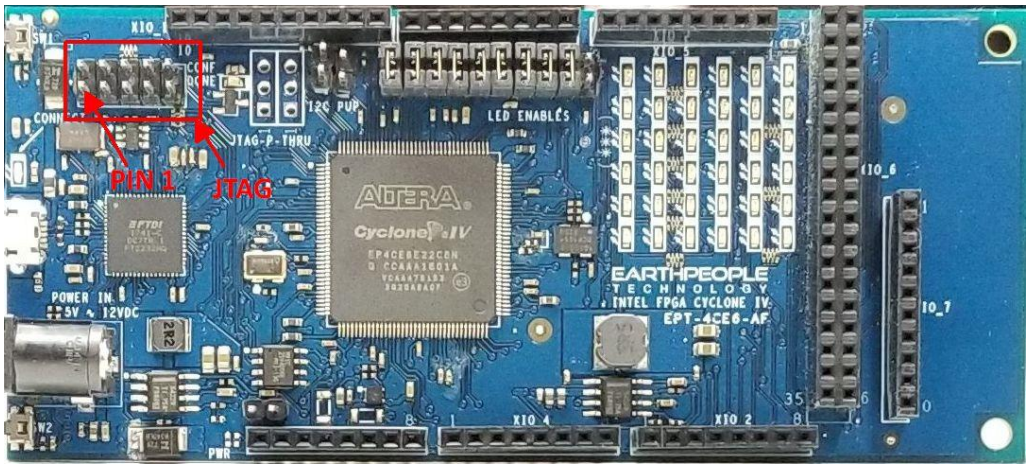
LED2	UB24	TBD	XIO_6 [2]
LED3	UB25	TBD	XIO_6 [3]
LED4	UB26	TBD	XIO_6[4]
LED5	UB27	TBD	XIO_6[5]
LED6	UB28	TBD	XIO_6[6]
LED7	UB29	TBD	XIO_6[7]
LED8	UB30	TBD	XIO_6 [8]
LED9	UB31	TBD	XIO_6 [9]
LED10	UB32	TBD	XIO_6 [10]
LED11	UB33	TBD	XIO_6 [11]
LED12	UB34	TBD	XIO_6[12]
LED13	UB35	TBD	XIO_6[13]
LED14	UB36	TBD	XIO_6[14]
LED15	UB37	TBD	XIO_6[15]
LED16	UB38	TBD	XIO_6 [16]
LED17	UB39	TBD	XIO_6 [17]
LED18	UB40	TBD	XIO_6 [18]
LED19	UB41	TBD	XIO_6 [19]
LED20	UB42	TBD	XIO_6[20]
LED21	UB43	TBD	XIO_6[21]
LED22	UB44	TBD	XIO_6[22]

LED23	UB45	TBD	XIO_6[23]
LED24	UB46	TBD	XIO_6 [24]
LED25	UB47	TBD	XIO_6 [25]
LED26	UB48	TBD	XIO_6 [26]
LED27	UB49	TBD	XIO_6 [27]
LED28	UB50	TBD	XIO_6[28]
LED29	UB51	TBD	XIO_6[29]
LED30	UB52	TBD	XIO_6[30]
LED31	UB53	TBD	XIO_6[31]
LED32	UB68	TBD	XIO_7[0]
LED33	UB69	TBD	XIO_7[1]
LED34	UB70	TBD	XIO_7[2]
LED35	UB71	TBD	XIO_7[3]

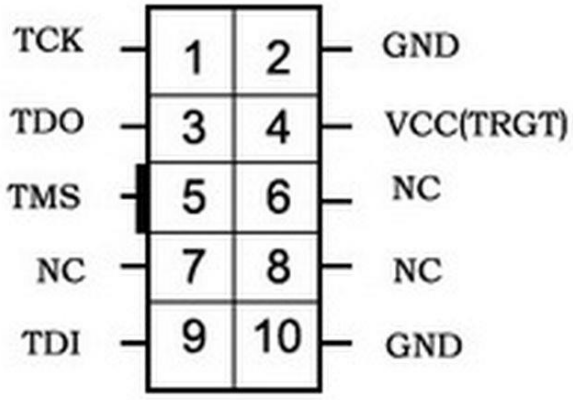


6 JTAG Header

A 10 pin, 5x2 connector is included on the DPL to provide JTAG programming of the Cyclone IV. The default programming method is via the Configuration Flash. JTAG programming the FPGA directly is provided as a secondary option. An external programmer must be used access this JTAG header. The header follows the standard Intel FPGA pinout. So, any USB Blaster compatible programmer can be used to connect directly to this header and program the FPGA. No other jumpers or configuration is needed, just connect the programmer and the Quartus software will recognize the FPGA.



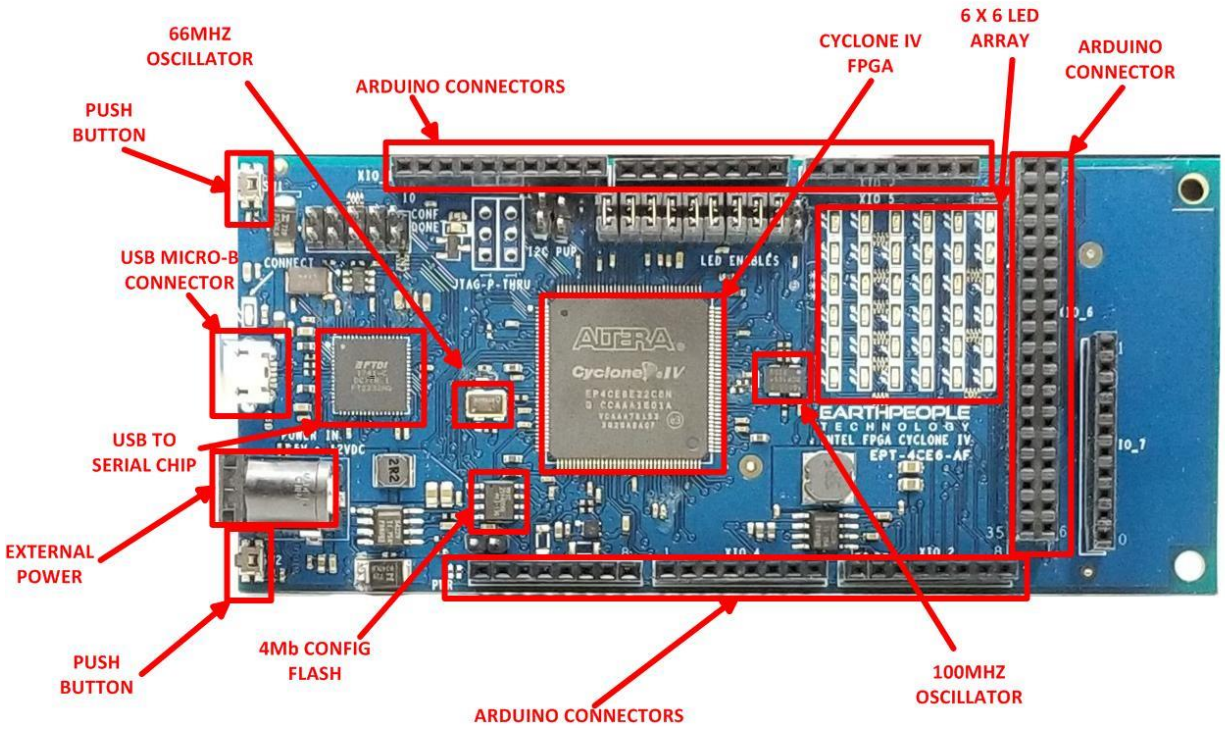
JTAG connector pinout:



7 Cyclone IV FPGA

The DueProLogic includes the Intel FPGA EP4CE6E22C8N, operating internally with 1.2V and 2.5V, and externally at 3.3V being 3.3V tolerant. Operates corner to corner logic in 9ns. 392 configurable logical/logic array blocks, 6272 logical elements/cells, 270Kbit internal RAM, 15 multipliers to support DSP processing-intensive applications, 2 PLLs.

8 Inputs/Outputs

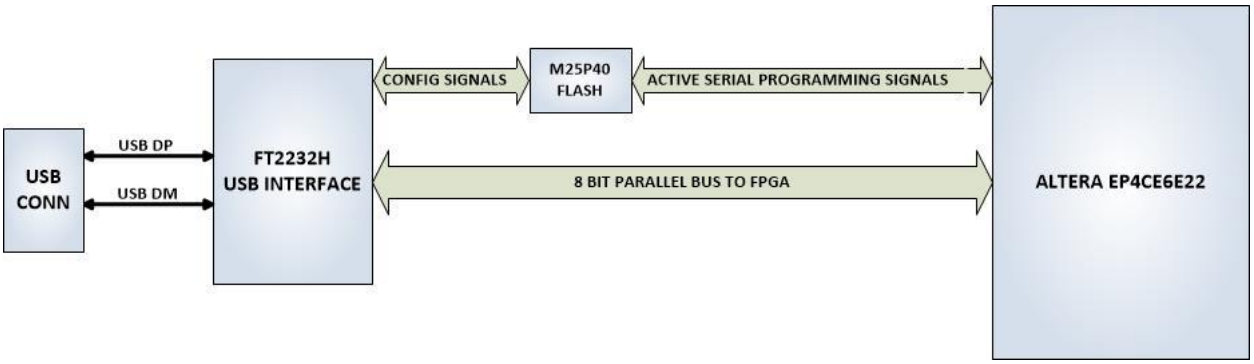


All I/O's are +3.3V only. Do not apply any voltage greater than +3.3V to the FPGA I/O's. All of the FPGA I/O's have been brought out to 0.1 inch socket/headers. These headers easily allow

jumper wire to connect from connector to the FPGA pins. Selected headers also have a power pin and a ground pin. This allows the user to assemble a small connector with both power and signals to connect to external sensor boards.

9 FPGA Configuration

The EPT Blaster Driver will allow the Quartus Prime Software to program the Configuration Flash chip on the DueProLogic. The software will only access the M25P40 Flash chip. This chip is accessed from the FT2232H USB chip. Quartus will store the compiled and synthesized user code. After programming is complete, the FPGA automatically resets and reads the code from the Flash chip and programs itself using the Active Serial method.



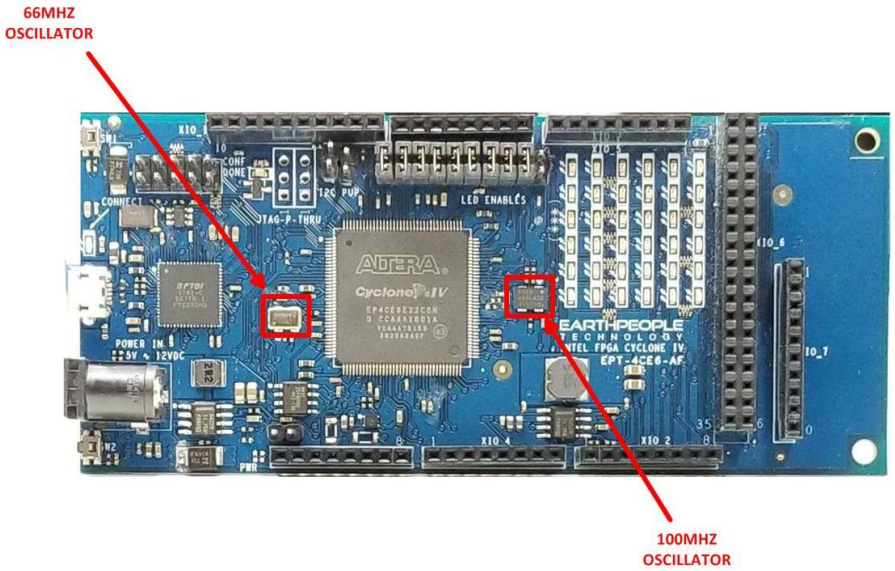
10 Oscillators

There are two oscillators on the DueProLogic, 66MHz and 100MHz. These oscillators have the following Vendor and P/N

1. 66MHz, Renesas Electronics America Inc; P/N: XLH536066.000000I
2. 100MHz, Renesas Electronics America Inc; P/N: XLH536100.000000I

These oscillators are connected to the Global Clock inputs on the FPGA. Both devices provide stable clock for the FPGA's internal DLL's. The user can access these clock sources by calling the net connected to the FPGA pin.

Component	Net Name	Pin on FPGA	Signal in EPT Project Pinout	
66MHz Osc	GCLK1	23	aa[1]	
100MHz Osc	GCLK7	88	CLK_100	



XLH536066.000000I

PARAMETERS	MAX (unless otherwise noted)
Frequency	66MHz
Supply Voltage (VDD)	3.3V

Input Current (IDD) >50.000 ~ 67.000MHz	25 mA
Standby Current	10 µA
Output Symmetry (50% VDD) >50.000 ~ 170.000MHz	40% ~ 60%
Rise/Fall Time (10%/90% VDD Levels) (TR/TF) 1.000 ~ 80.000MHz	6 nS
Output Voltage (VOL) (VOH)	10% VDD 90% VDD Min
Output Load (HCMOS)	15 pF
Start-up Time (TS)	10 mS
Frequency Stability	±25ppm
Operating Temperature	-40°C ~ 85°C

XLH536100.000000I

PARAMETERS	MAX (unless otherwise noted)
Frequency	100MHz
Supply Voltage (VDD)	3.3V

Input Current (IDD) >50.000 ~ 67.000MHz	47 mA
Standby Current	10 µA
Output Symmetry (50% VDD) >50.000 ~ 170.000MHz	40% ~ 60%
Rise/Fall Time (10%/90% VDD Levels) (TR/TF) 1.000 ~ 80.000MHz	6 nS
Output Voltage (VOL) (VOH)	10% VDD 90% VDD Min
Output Load (HCMOS)	15 pF
Start-up Time (TS)	10 mS
Frequency Stability	±25ppm
Operating Temperature	-40°C ~ 85°C

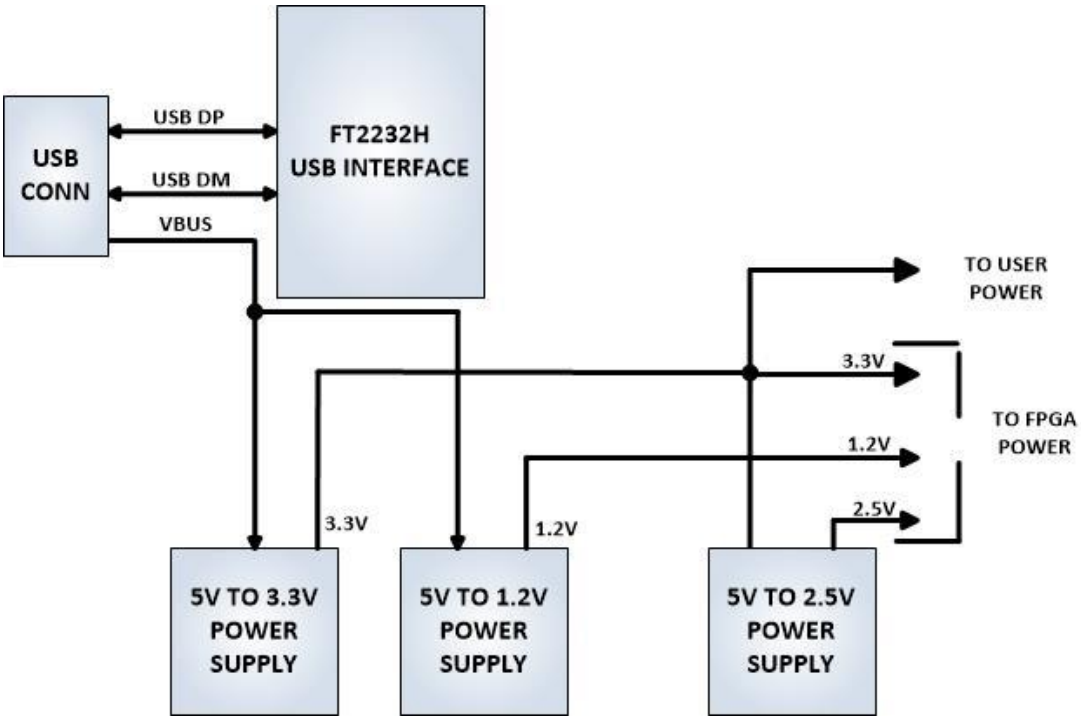
11 USB to Serial

The FT2232HQ is a USB 2.0 High Speed (480Mb/s) to UART/MPSSE IC. The device features two interfaces that can be configured for asynchronous or synchronous serial or parallel FIFO interfaces. The two channels can also be independently configured to use an MPSSE engine. This allows the two ports of the FT2232HQ to operate independently as UART/Bit-Bang ports or MPSSE engines used to emulate JTAG, SPI, I2C, Bit-bang or other synchronous serial modes.

The chip is powered by +3.3V and includes an internal +1.8V regulator to power the chip core. It uses +3.3V I/O interfacing and is+5V Tolerant. Operational configuration mode and USB Description strings configurable in external EEPROM over the USB interface. USB to parallel FIFO transfer data rate up to 8 Mbyte/Sec. FT245B-style FIFO interface option with bi-directional data bus and simple 4 wire handshake interface. Asynchronous serial UART interface option with full hardware handshaking and modem interface signals. Fully assisted hardware or X-On / X-Off software handshaking. UART Interface supports 7/8 bit data, 1/2 stop bits, and Odd/Even/Mark/Space/No Parity.

12 DueProLogic Power

The DueProLogic can be powered from the USB bus of a Host/PC or the optional barrel connector. The USB supplies a maximum of +5V @ 500mA's. The components of the DueProLogic must share this power with the user code that will run inside the FPGA along with any external power use.



12.1 Core Board Power Budget

Device	**Part Number**	**+1.2V Power**	**+2.5V Power**	**+3.3V Power**
FPGA	EP4CE6E22	??? Defined by user code. EPT-Transfer-Demo code: 50mA	10mA	??? Defined by user code. . EPT-Transfer-Demo code: 50mA

Flash	M25P40			15mA (During the Write Status, Sector Erase, and Bulk Erase cycles)
USB Chip	FT2232H			60 mA (no sink current supplied to I/O's)
USB EEPROM	93LC56			2 mA (write current) 1 mA (read current)
66MHz Oscillator	FXO-HC536R-66			47 mA
100MHz Oscillator	FXO-HC536R-100			47 mA
User LEDs				216 mA
CONF_DONE Green LED				5 mA
CONNECT Green LED				5mA
Total		**50mA**	**10mA**	**261mA**

*Theoritical Values only. This data needs to be validated

12.2 Core Board VUSB Power Budget

Device	**Part Number**	**VUSB**		
+1.2V Power Supply	ISL9205IRZ	70mA		
+2.5V Power Supply	NCP360MU	12mA		
+3.3V Power Supply	LTC2952	275mA		
Total		**357mA**		

* Theoritical Values only. This data needs to be validated