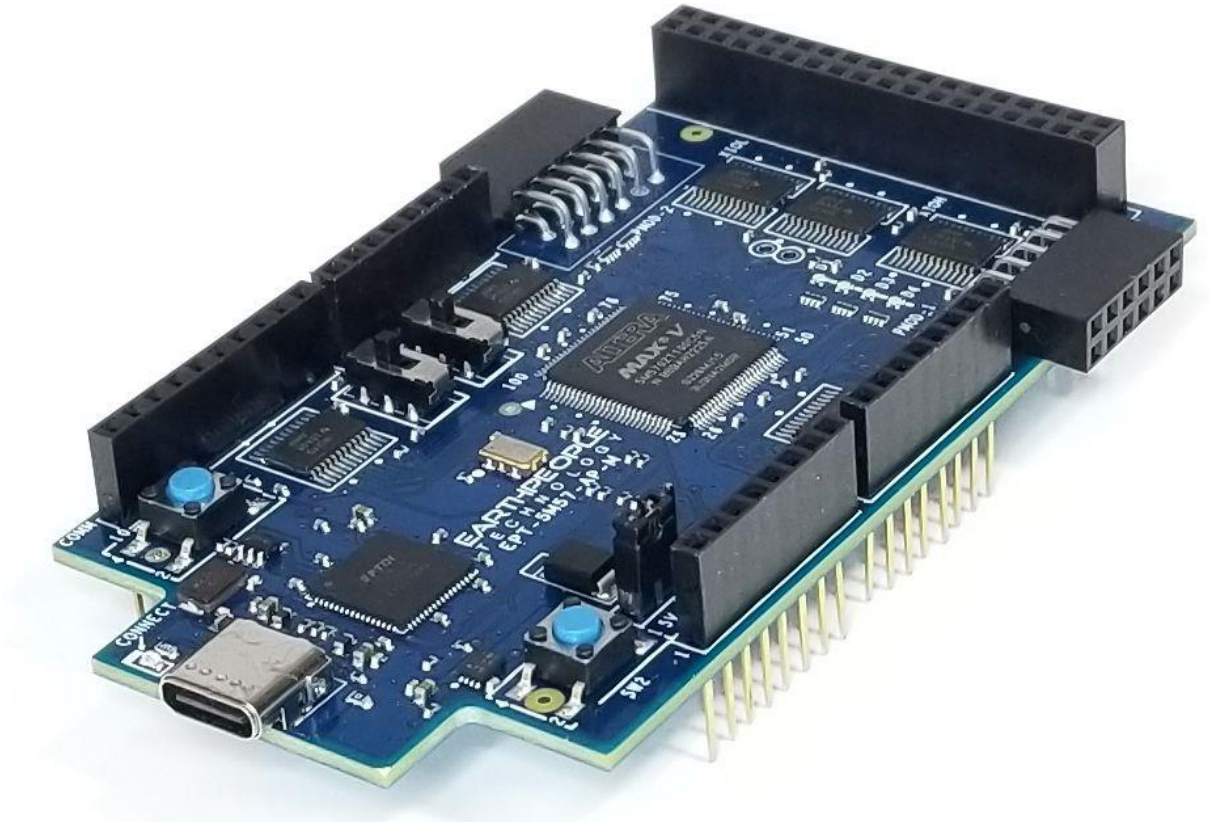
MEGAPROLOGIC

USB PLD DEVELOPMENT SYSTEM

Data Sheet



The MegaProLogic is a part of the EPT USB/PLD development system. It provides an innovative method of developing and debugging the users microcontroller code. It can also provide a high speed data transfer mechanism between microcontroller and Host PC.

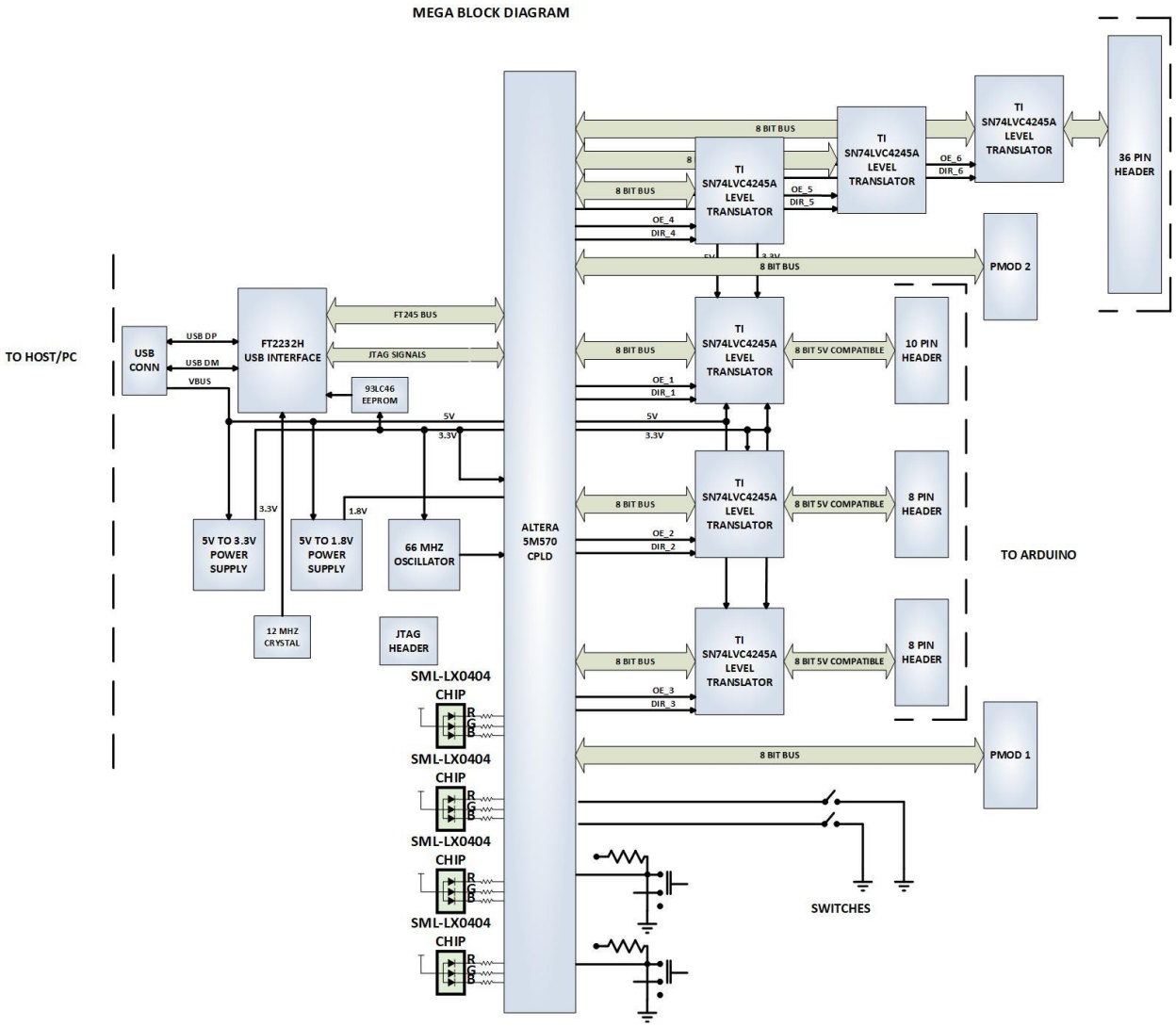
The MegaProLogic board is equipped with an Altera 5M570 PLD; which is programmed using

the Intel Quartus Prime software. The CPLD has 570 Logic Elements which is equivalent to 440 Macrocells. An on board 66 MHz oscillator is used by the EPT-Active-Transfer-Library to provide data transfer rates of 0.1 Mega Bytes per second. The EPT-Active-Transfer-Library provides control communication between the objective device and the CPLD. Data transfer during the objective device checkout between the PC and the CPLD program is available via the Hyper Serial Port. The board also includes the following parts.

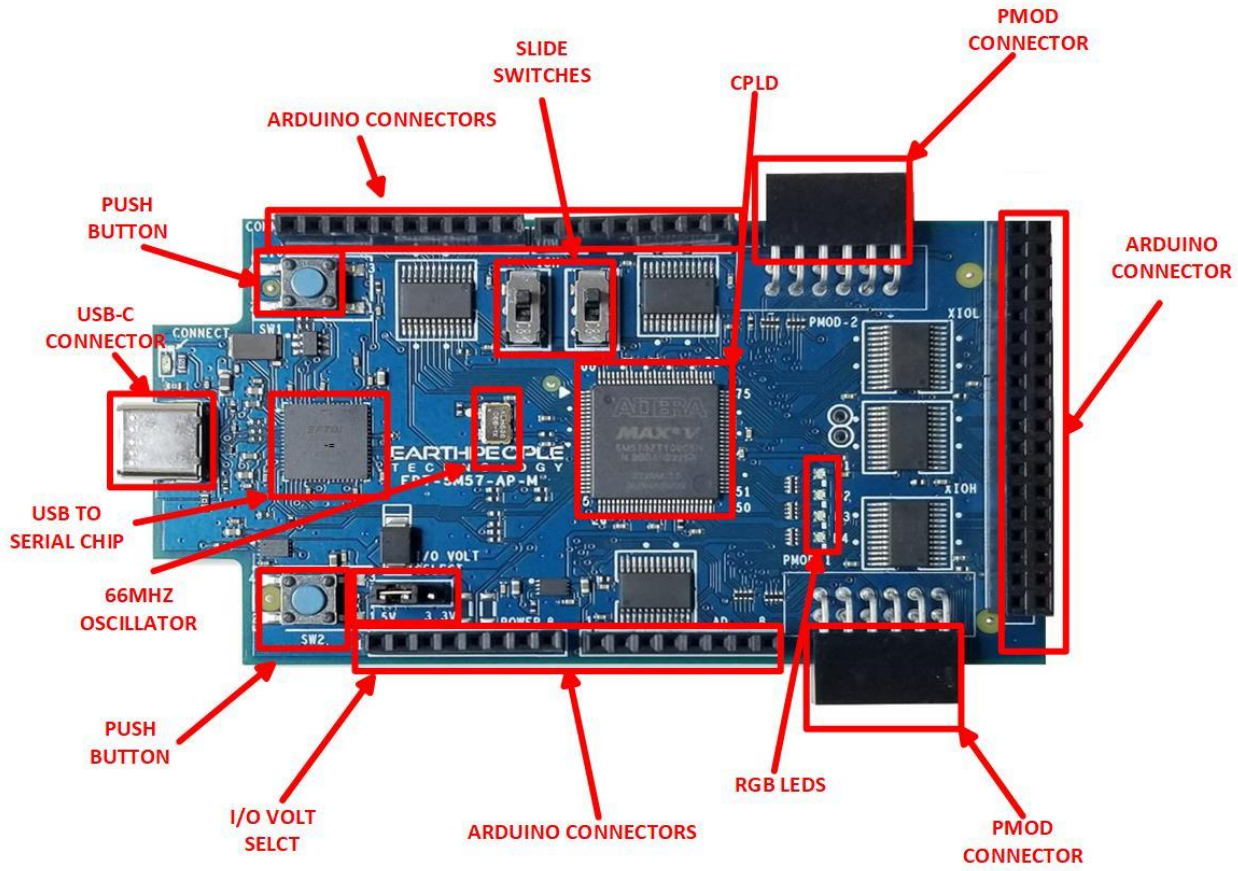
- Altera 5M570 in the TQFP 100 pin package
- 66 MHz oscillator for driving USB data transfers and users code
- Four 74LVC245 bidirectional voltage translator/bus transceiver
- 32 user Input/Outputs
- Four RGB LED's accessible by the user
- Two PCB switches accessible by the user
- Two Slide switches accessible by the user
- All connectors to stack into the Arduino Uno
- USB to Serial FT2232H Dual Channel Chip

User Manual EPT USB PLD Dev Sys For The MEGA

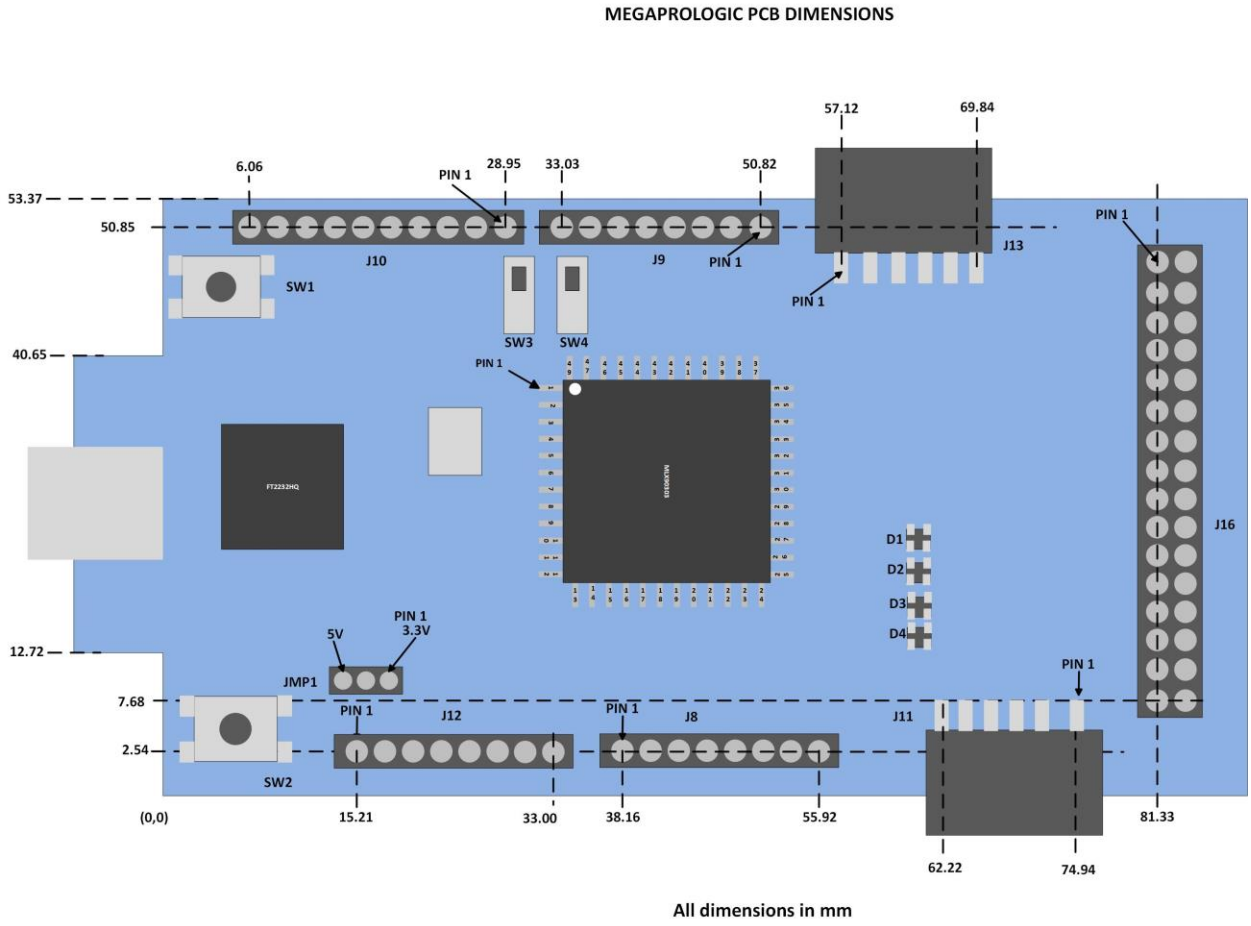
1 Block Diagram



User Manual EPT USB PLD Dev Sys For The MEGA



2 Mechanical Dimensions



3 Pin Mapping

Pin Mapping between Connectors, MAXV CPLD and User code

J10 Connector

MegaPrologic Connector-Pin #	MegaPrologic Net Name	MegaPrologic CPLD Pin Number	MegaPrologic CPLD User Code Signal Name
J10-1	LB0	1	LB_COMM[0]
J10-2	LB1	2	LB_COMM [1]

J10-3	LB2	3	LB_COMM [2]
J10-4	LB3	4	LB_COMM [3]
J10-5	LB4	5	LB_COMM [4]
J10-6	LB5	6	LB_COMM [5]
J10-7	LB6	7	LB_COMM[6]
J10-8	LB7	15	LB_COMM[7]
J10-9	NC	NC	NC
J10-10	NC	NC	NC

J8 Connector

MegaPrologic Connector-Pin #	**MegaPrologic Net Name**	**MegaPrologic CPLD Pin Number**	**MegaPrologic CPLD User Code Signal Name**
J8-1	LB8	33	LB_AD [0]
J8-2	LB9	34	LB_AD [1]
J8-3	LB10	35	LB_AD [2]
J8-4	LB11	36	LB_AD [3]
J8-5	LB12	38	LB_AD [4]
J8-6	LB13	40	LB_AD [5]
J8-7	LB14	41	LB_AD [6]
J8-8	LB15	42	LB_AD [7]

J9 Connector

MegaPrologic Connector-Pin #	**MegaPrologic Net Name**	**MegaPrologic CPLD Pin Number**	**MegaPrologic CPLD User Code Signal Name**
J9-1	LB16	87	LB_IOH [0]
J9-2	LB17	89	LB_IOH [1]
J9-3	LB18	91	LB_IOH [2]
J9-4	LB19	92	LB_IOH [3]
J9-5	LB20	96	LB_IOH [4]
J9-6	LB21	97	LB_IOH [5]
J9-7	LB22	98	LB_IOH [6]
J9-8	LB23	99	LB_IOH [7]

J16 Connector

MegaPrologic Connector-Pin #	MegaPrologic Net Name	MegaPrologic CPLD Pin Number	MegaPrologic CPLD User Code Signal Name
J16-1	NC	NC	NC
J16-2	NC	NC	NC
J16-3	LB38 & CIO_A_6	83	LB_IOLA [6]
J16-4	LB39 & CIO_A_7	84	LB_IOLA [7]
J16-5	LB36 & CIO_A_4	81	LB_IOLA [4]
J16-6	LB37 & CIO_A_5	82	LB_IOHA [3]
J16-7	LB34 & CIO_A_2	77	LB_IOLA [2]
J16-8	LB35 & CIO_A_3	78	LB_IOLA [3]
J16-9	LB32 & CIO_A_0	75	LB_IOLA [0]
J16-10	LB33 & CIO_A_1	76	LB_IOLA [1]
J16-11	NC	NC	
J16-12	NC	NC	
J16-13	NC	NC	
J16-14	NC	NC	

J16-15	NC	NC	
J16-16	NC	NC	
J16-17	NC	NC	
J16-18	NC	NC	
J16-19	LB46 & CIO_C_6	NC	TP1
J16-20	LB47 & CIO_C_7	NC	TP2
J16-21	SW_USER_1 & CIO_C_4	NC	SW1
J16-22	SW_USER_2 & CIO_C_5	NC	SW2
J16-23	LB42 & CIO_C_2	72	LB_IOLC [2]
J16-24	LB43 & CIO_C_3	44	RST
J16-25	LB40 & CIO_C_0	70	LB_IOLC [0]
J16-26	LB41 & CIO_C_1	71	LB_IOLC [1]
J16-27	LB31 & CIO_D_7	69	LB_IOH [7]
J16-28	LB30 & CIO_D_6	68	LB_IOH [6]

J16-29	LB29 & CIO_D_5	67	LB_IOH [5]
J16-30	LB28 & CIO_D_4	66	LB_IOH [4]
J16-31	LB27 & CIO_D_3	64	LB_IOH [3]
J16-32	LB26 & CIO_D_2	62	LB_IOH [2]
J16-33	LB25 & CIO_D_1	61	LB_IOH [1]
J16-34	LB24 & CIO_D_0	58	LB_IOH [0]
J16-35	GND	NC	
J16-36	GND	NC	

Net Name Mapping between components

Component	**Pin**	**Net Name**	**Pin on CPLD**	**Signal in EPT Project Pinout**
66MHz Oscillator	3	GCLK	12	CLK_66MHZ
Reset	2	NA	44	RST
U1	16	AD0	24	JTAG_TCK (Not In Project)
	17	AD1	23	JTAG_TDI (Not In Project)
	18	AD2	25	JTAG_TDO (Not In Project)
	19	AD3	22	JTAG_TMS (Not In Project)

	38	BD0	19	UART_IN
	39	BD1	18	UART_OUT
SLIDE_SWITCH_2	1	SLIDE_SWITCH_2	17	SLIDE_SWITCH_2
SLIDE_SWITCH_1	1	SLIDE_SWITCH_1	16	SLIDE_SWITCH_1
U7	14	LB7	15	LB_COMM 7
	15	LB6	7	LB_COMM 6
	16	LB5	6	LB_COMM 5
	17	LB4	5	LB_COMM 4
	18	LB3	4	LB_COMM 3
	19	LB2	3	LB_COMM 2
	20	LB1	2	LB_COMM 1
	21	LB0	1	LB_COMM 0
SW1	1	SW_USER_1	20	SW_USER_1
SW2	1	SW_USER_2	21	SW_USER_23
U7	2	TR_DIR_1	100	TR_DIR_1
U4	2	TR_DIR_2	29	TR_DIR_2
U5	2	TR_DIR_3	85	TR_DIR_3
U15	2	TR_DIR_4	30	TR_DIR_4
U13	2	TR_DIR_5	27	TR_DIR_5
U7	22	TR_OE_1	86	TR_OE_1
U4	22	TR_OE_2	28	TR_OE_2
U5	22	TR_OE_3	74	TR_OE_3
U15	22	TR_OE_4	73	TR_OE_4
U13	22	TR_OE_5	26	TR_OE_5
D2	1	LED_GR_2_N	54	LED_GR_2
	2	LED_BL_2_N	53	LED_BL_2
	3	LED_RD_2_N	52	LED_RD_2
D3	1	LED_GR_3_N	51	LED_GR_3
	2	LED_BL_3_N	50	LED_BL_3
	3	LED_RD_3_N	49	LED_RD_3
D4	1	LED_GR_4_N	48	LED_GR_4
	2	LED_BL_4_N	47	LED_BL_4
	3	LED_RD_4_N	43	LED_RD_4
D1	1	LED_GR_1_N	57	LED_GR_1
	2	LED_BL_1_N	56	LED_BL_1

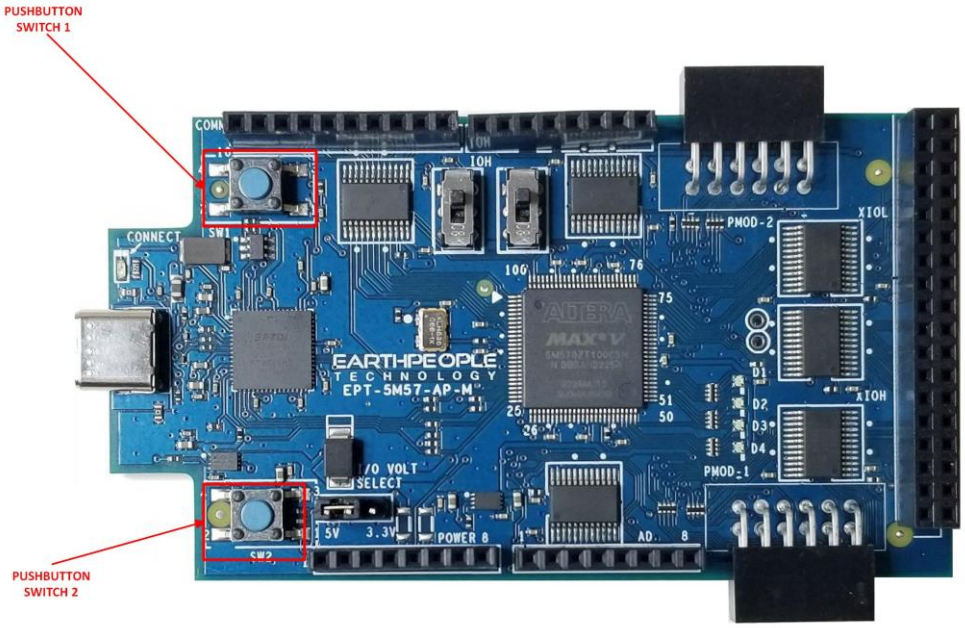
	3	LED_RD_1_N	55	LED_RD_1
U4	21	LB8	33	LB_AD0
	20	LB9	34	LB_AD1
	19	LB10	35	LB_AD2
	18	LB11	36	LB_AD3
	17	LB12	38	LB_AD4
	16	LB13	40	LB_AD5
	15	LB14	41	LB_AD6
	14	LB15	42	LB_AD7
U5	21	LB16	87	LB_IOH0
	20	LB17	89	LB_IOH1
	19	LB18	91	LB_IOH2
	18	LB19	92	LB_IOH3
	17	LB20	96	LB_IOH4
	16	LB21	97	LB_IOH5
	15	LB22	98	LB_IOH6
	14	LB23	99	LB_IOH7
U13	21	LB24	58	LB_XIOH 0
	20	LB25	61	LB_XIOH 1
	19	LB26	62	LB_XIOH 2
	18	LB27	64	LB_XIOH 3
	17	LB28	66	LB_XIOH 4
	16	LB29	67	LB_XIOH 5
	15	LB30	68	LB_XIOH 6
	14	LB31	69	LB_XIOH 7
U15	21	LB32	75	LB_XIOLA 0
	20	LB33	76	LB_XIOLA 1
	19	LB34	77	LB_XIOLA 2
	18	LB35	78	LB_XIOLA 3
	17	LB36	81	LB_XIOLA 4
	16	LB37	82	LB_XIOLA 5
	15	LB38	83	LB_XIOLA 6
	14	LB39	84	LB_XIOLA 7
U14	21	LB40	70	LB_XIOLC 0
	20	LB41	71	LB_XIOLC 1

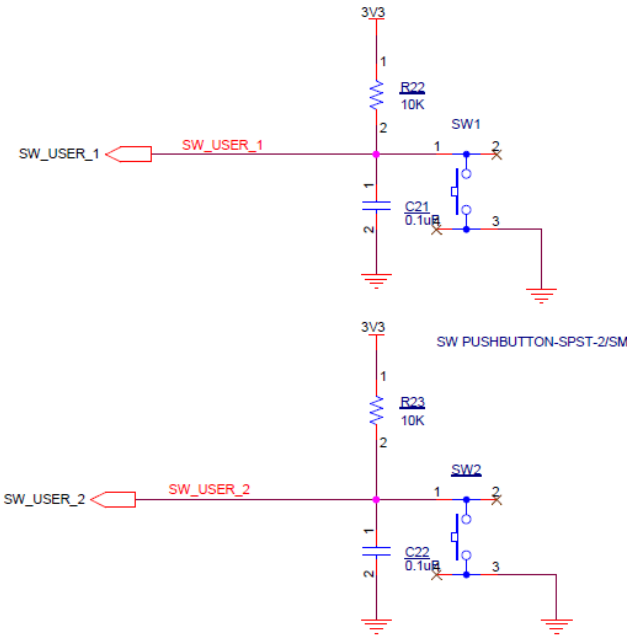
	19	LB42	72	LB_XIOLC 2
	18	LB43	44	RST

4 Pushbutton switches

There are two pushbutton switches on the MegaProLogic. Both are momentary contact switches. They include a 1uF cap to ground to debounce both switches.

Component	Net Name	Pin on CPLD	Signal in EPT Project Pinout
SW1	SW_USER_1	20	SW_USER_1
SW2	SW_USER_2	21	SW_USER_23

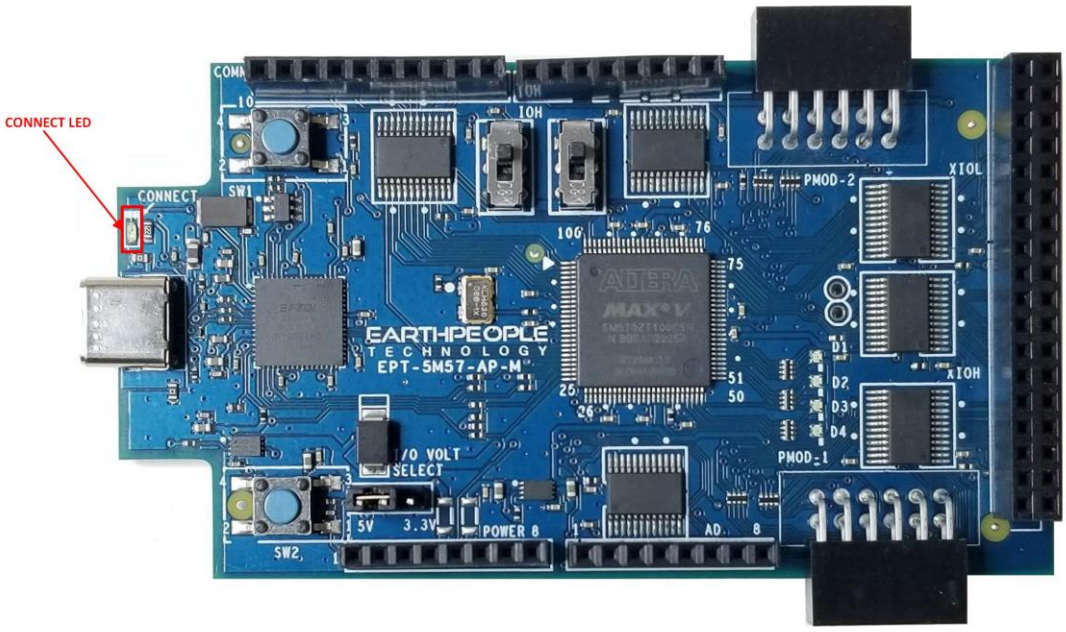




4.1.1 Host PC Connection

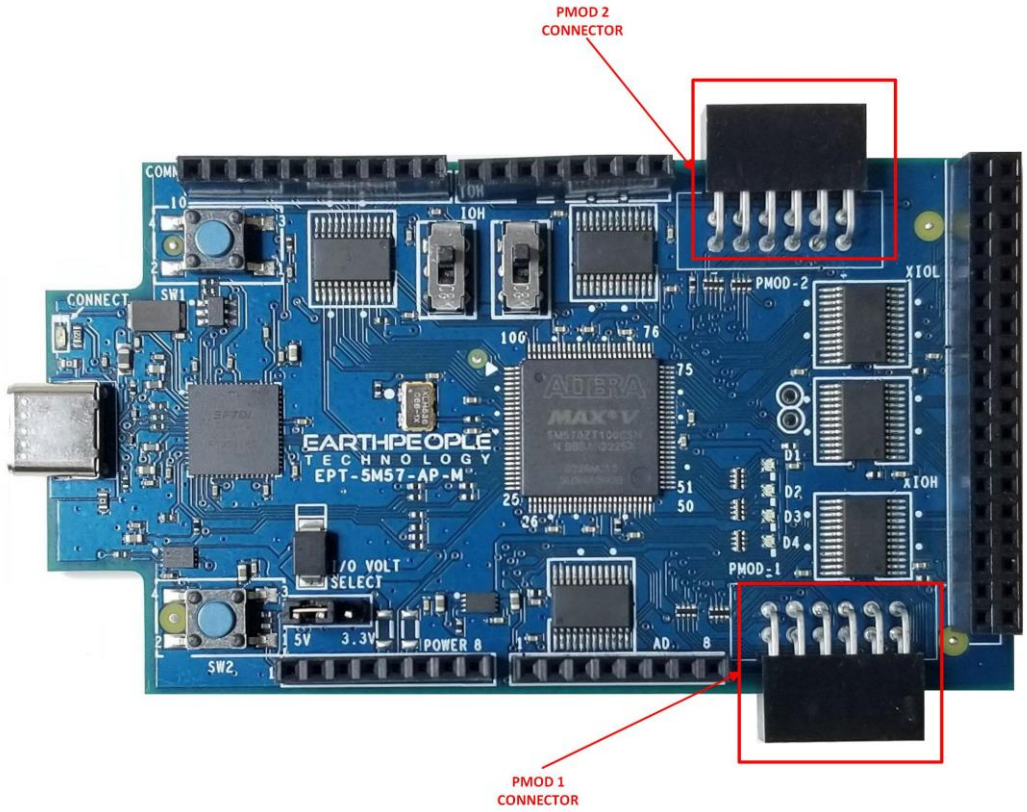
The MegaProLogic includes an LED that signifies the connection of the board with the Host PC. The connect LED has the word “CONNECT” in silkscreen next to the LED. This LED will only light up once the Host PC has correctly enumerated the USB device (FT2232HQ chip). When this LED is lit up it can tell the user three things:

- Power has been applied to the MegaProLogic via USB
- The FT2232HQ chip is working properly
- The Host PC has found the appropriate driver and will communicate with the MegaProLogic

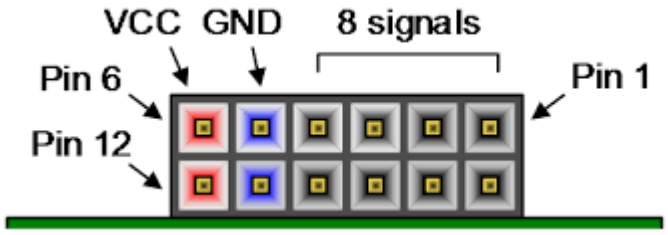


4.1.2 PMOD Connectors

The MegaProLogic includes two PMOD Connectors. These two connectors are located towards the rear of the board.

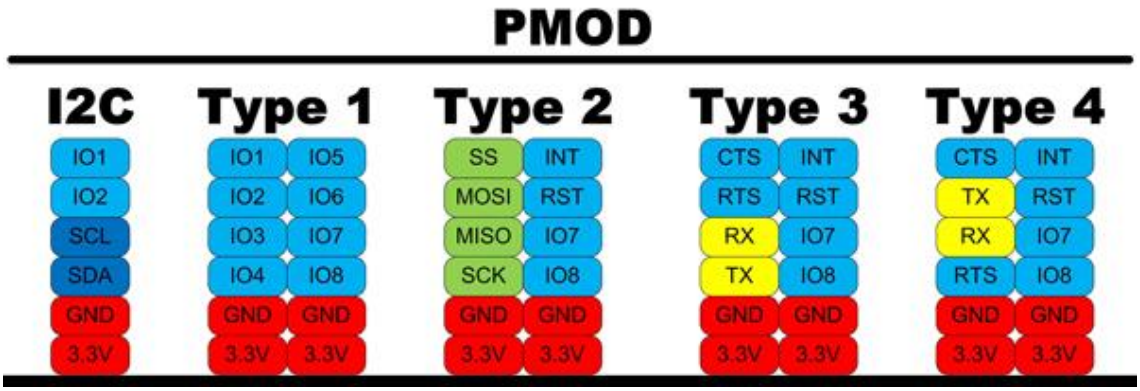


The PMOD pinouts follows the standard pinout. Pin 1 is located in the upper right when facing the connector.



VCC is +3.3V and the Inputs and Outputs of the 8 signals are +3.3V only. The eight I/O's are connected

directly to FPGA pins and can be designated as any communications standard.



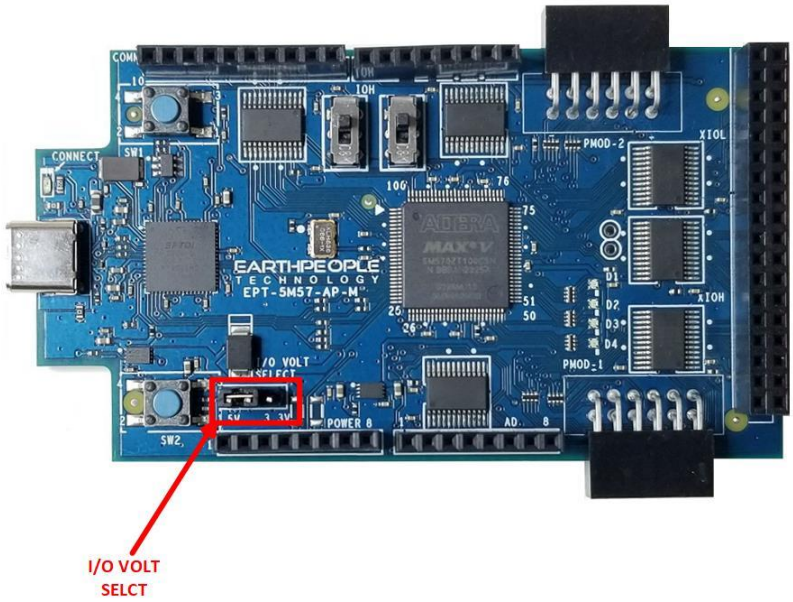
The PMOD have the following connections to the MAX V chip:

PMOD Pin Number	Signal Name	MAX V Pin Number
1-1	LB31	69
1-2	LB29	67
1-3	LB27	64
1-4	LB25	61
1-7	LB30	68
1-8	LB28	66
1-9	LB26	62
1-10	LB24	58
2-1	LB39	84
2-2	LB37	82
2-3	LB35	78
2-4	LB33	76
2-7	LB38	83
2-8	LB36	81

2-9	LB34	77
2-10	LB32	75

4.1.3 Inputs and Outputs

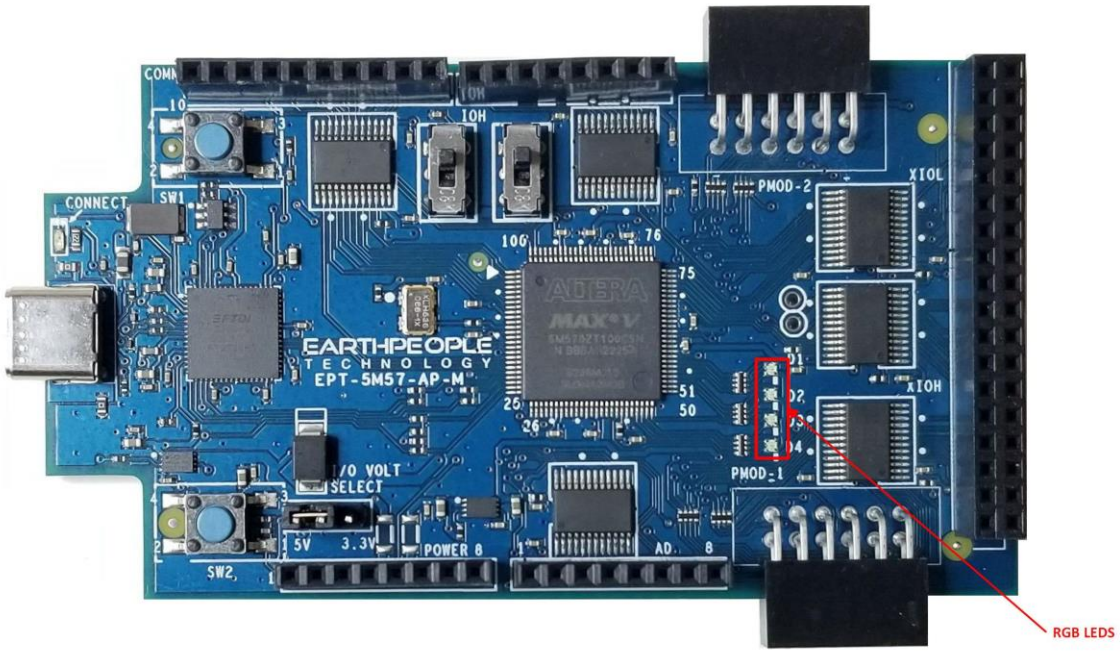
There are 32 Inputs/Outputs which are selectable between +3.3V and +5 Volt. JMP1 is used to select which voltage the 32 Inputs/Outputs are set to.



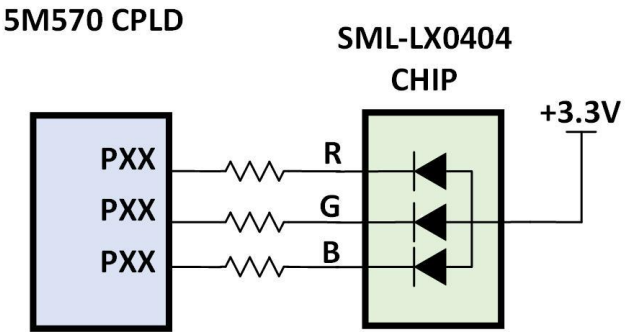
The I/O's are organized as three 8 bit directional ports. Each port must be defined as input or output. This means that all 8 bits of a port will point in the same direction, depending on the direction bit of the transceiver. The direction bit can be changed at any time, so that a port can change from input to output in minimum setup time of 6 nanoseconds. Each port also has an enable pin. This enable pin will enable or disable the bits of the port. If the port is disabled, the bits will "float".

4.1.4 User LEDs

The User LEDs are four RGB LEDs. These LEDs are SML-LX0404 chips and are for use only with +3.3V.



The SML-LX0404 chip is a current sink and are connected to pins on the MAX V CPLD. The anode is connected to +3.3V. The series resistors are calculated for current limiting based on +3.3V.



Each series resistor uses a 220 Ohm in a resistor array. In order to light up the each LED, the user code must assert a zero on the associated signal for the LED. To turn off the LED, assert High Z on the signal.

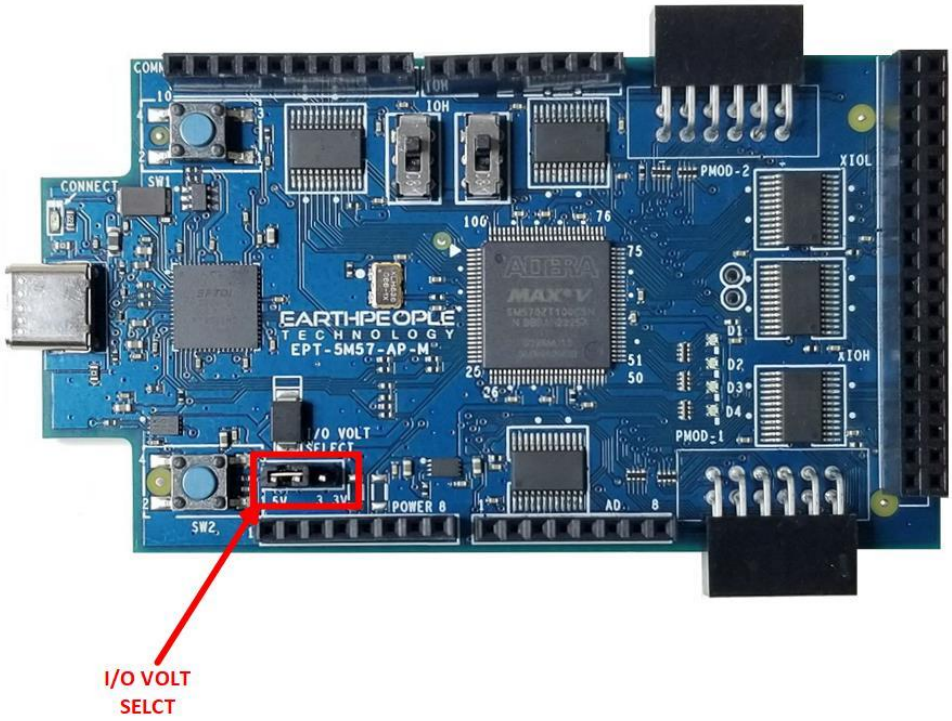
The LED RGB signals are organized on the following pins from the MAX V chip:

LED Number	Signal Name	MAX V Pin Number
D1	LED_GREEN_1_N	57
D1	LED _BLUE_1_N	56
D1	LED_RED_1_N	55
D2	LED_GREEN_2_N	54
D2	LED _BLUE_2_N	53
D2	LED_RED_2_N	52
D3	LED_GREEN_3_N	51
D3	LED _BLUE_3_N	50
D3	LED_RED_3_N	49
D4	LED_GREEN_4_N	48
D4	LED _BLUE_4_N	47
D4	LED_RED_4_N	43

5 Inputs/Outputs

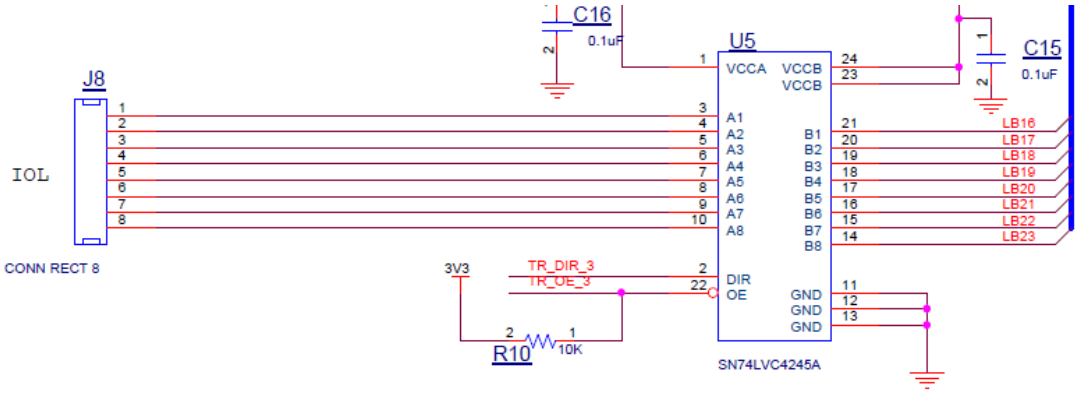
The UnoMax is designed from the ground up as a development board for beginners. All of the Inputs/Outputs are protected by the 74LVC8245 transceiver chips. These transceivers provide both voltage level translations and protection from over current and over voltage. The transceivers can sink up to 50mA per pin.

There are 24 Inputs/Outputs which are selectable between +3.3V and +5 Volt. JMP1 is used to select which voltage the 24 Inputs/Outputs are set to.



The I/O's are organized as three 8 bit directional ports. Each port must be defined as input or output. This means that all 8 bits of a port will point in the same direction, depending on the direction bit of the transceiver. The direction bit can be changed at any time, so that a port can

change from input to output in minimum setup time of 6 nanoseconds. Each port also has an enable pin. This enable pin will enable or disable the bits of the port. If the port is disabled, the bits will “float”.



This 8-bit (octal) noninverting bus transceiver contains two separate supply rails; B port has VCCB, which is set at 3.3 V, and A port has VCCA, which is set at 5 V. This allows for translation from a 3.3-V to a 5-V environment, and vice versa.

The SN74LVC4245A device is designed for asynchronous communication between data buses. The device transmits data from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable (OE) input can be used to disable the device so the buses are effectively isolated. The control circuitry (DIR, OE) is powered by VCCA.

5.1 Electrical Characteristics

for V_{CCA} = 4.5 V to 5.5 V(1)

		MIN	MAX	UNIT
V_{CCA}	Supply voltage	4.5	5.5	V
V_{IH}	High-level input voltage	2		V
V_{IL}	Low-level input voltage		0.8	V
V_{IA}	Input voltage	0	V_{CCA}	V
V_{OA}	Output voltage	0	V_{CCA}	V
I_{OH}	High-level output current		–24	mA
I_{OL}	Low-level output current		24	mA
T_A	Operating free-air temperature	–40	85	°C

(1) All unused inputs of the device must be held at the associated V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

Tim

for V_{CCB} = 2.7 V to 3.6 V(1)

			MIN	MAX	UNIT
V_{CCB}	Supply voltage		2.7	3.6	V
V_{IH}	High-level input voltage	V_{CCB} = 2.7 V to 3.6 V	2		V
V_{IL}	Low-level input voltage	V_{CCB} = 2.7 V to 3.6 V		0.8	V
V_{IB}	Input voltage		0	V_{CCB}	V
V_{OB}	Output voltage		0	V_{CCB}	V
I_{OH}	High-level output current	V_{CCB} = 2.7 V		–12	mA
		V_{CCB} = 3 V		–24	
I_{OL}	Low-level output current	V_{CCB} = 2.7 V		12	mA
		V_{CCB} = 3 V		24	
T_A	Operating free-air temperature		–40	85	°C

(1) All unused inputs of the device must be held at the associated V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

5.2 Timing Characteristics

over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCA} = 5 V ± 0.5 V, V_{CCB} = 2.7 V to 3.6 V		UNIT
			MIN	MAX	
t_{PHL}	A	B	1	6.3	ns
t_{PLH}			1	6.7	
t_{PHL}	B	A	1	6.1	ns
t_{PLH}			1	5	
t_{PZL}	$\overline{OE}$	A	1	9	ns
t_{PZH}			1	8.1	
t_{PZL}	$\overline{OE}$	B	1	8.8	ns
t_{PZH}			1	9.8	
t_{PLZ}	$\overline{OE}$	A	1	7	ns
t_{PHZ}			1	5.8	
t_{PLZ}	$\overline{OE}$	B	1	7.7	ns
t_{PHZ}			1	7.8	

5.3 Description

24 mA drive at 3-V supply
– Good for heavier loads and longer traces
Low VIH
– Allows 3.3-V to 5-V translation

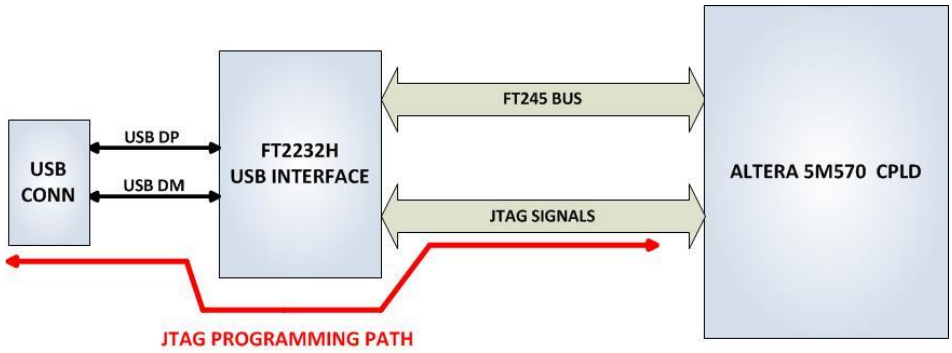
Function Table

INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

6 MAXV Programming

The UnoMax uses the second channel of the FT2232H chip as a dedicated CPLD programming port. The CPLD must be programmed via JTAG signals and the FT2232H has built in JTAG

signals.



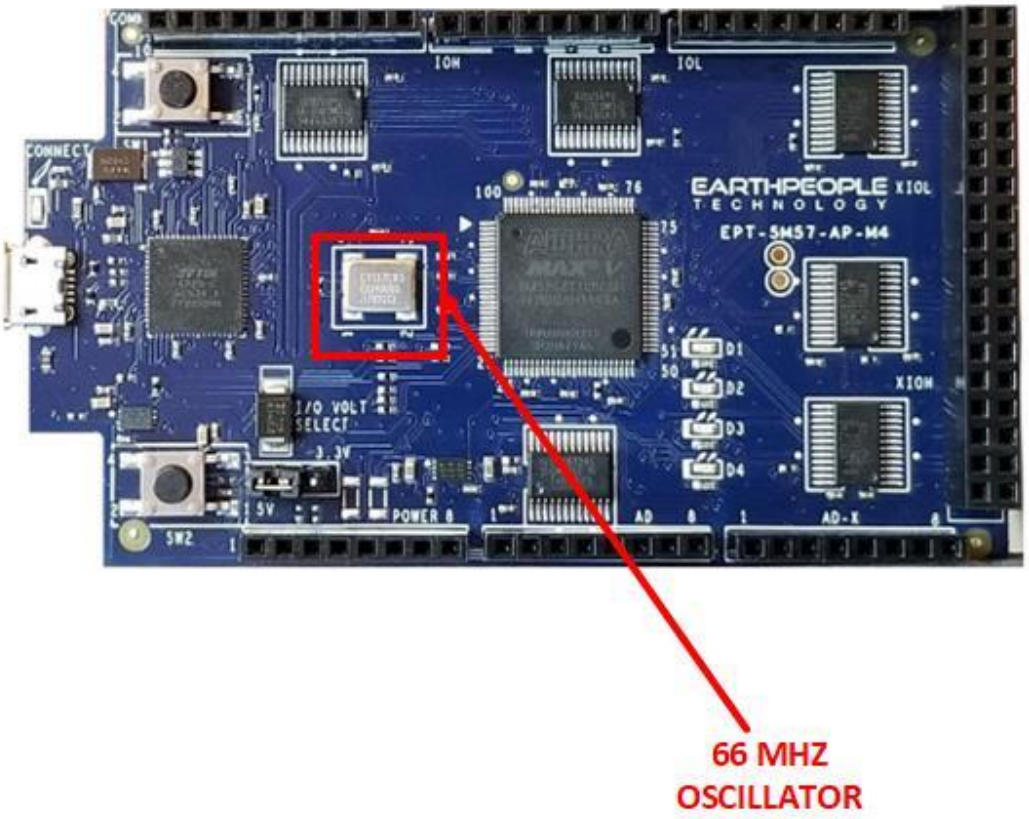
7 Oscillator

There is a 66MHz oscillator on the MegaProLogic, This oscillator has the following Vendor and P/N

1. 66MHz, Renesas Electronics America Inc; P/N: XLH536066.000000I

This oscillators are connected to the Global Clock inputs on the FPGA. Both devices provide stable clock for the FPGA's internal DLL's. The user can access these clock sources by calling the net connected to the FPGA pin.

Component	Net Name	Pin on CPLD	Signal in EPT Project Pinout	
66MHz Osc	GCLK1	23	CLK_66MHZ	



XLH536066.000000I

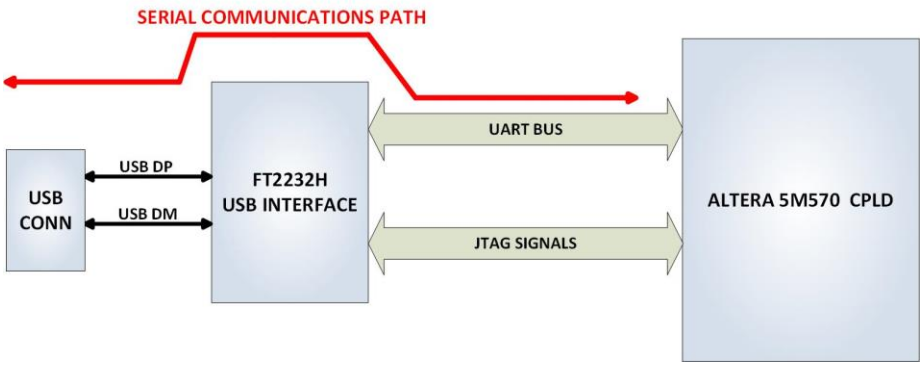
PARAMETERS	MAX (unless otherwise noted)
Frequency	66MHz
Supply Voltage (VDD)	3.3V
Input Current (IDD) >50.000 ~ 67.000MHz	25 mA
Standby Current	10 µA
Output Symmetry (50% VDD) >50.000 ~ 170.000MHz	40% ~ 60%

Rise/Fall Time (10%/90% VDD Levels) (TR/TF) 1.000 ~ 80.000MHz	 6 nS
Output Voltage (VOL) (VOH)	10% VDD 90% VDD Min
Output Load (HCMOS)	15 pF
Start-up Time (TS)	10 mS
Frequency Stability	±25ppm
Operating Temperature	-40°C ~ 85°C

8 USB to Serial

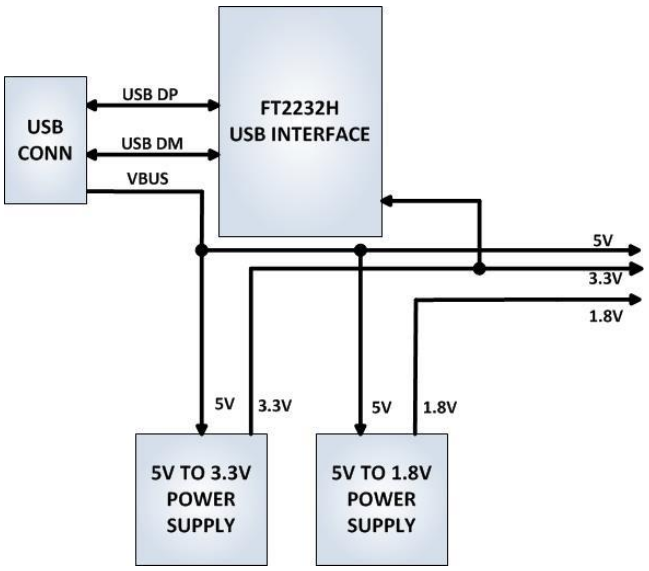
The FT2232HQ is a USB 2.0 High Speed (480Mb/s) to UART/MPSSE IC. The device features two interfaces that can be configured for asynchronous or synchronous serial or parallel FIFO interfaces. The two channels can also be independently configured to use an MPSSE engine. This allows the two ports of the FT2232HQ to operate independently as UART/Bit-Bang ports or MPSSE engines used to emulate JTAG, SPI, I2C, Bit-bang or other synchronous serial modes.

The chip is powered by +3.3V and includes an internal +1.8V regulator to power the chip core. It uses +3.3V I/O interfacing and is+5V Tolerant. Operational configuration mode and USB Description strings configurable in external EEPROM over the USB interface. Asynchronous serial UART interface option with full hardware handshaking and modem interface signals. Fully assisted hardware or X-On / X-Off software handshaking. UART Interface supports 7/8 bit data, 1/2 stop bits, and Odd/Even/Mark/Space/No Parity.



9 MegaProLogic Power

The MegaProLogic can be powered from the USB bus of a Host/PC or the optional barrel connector. The USB supplies a maximum of +5V @ 500mA's. The components of the MegaProLogic must share this power with the user code that will run inside the CPLD along with any external power use.



9.1 Core Board Power Budget

Device	Part Number	+1.8V Power	+3.3V Power
CPLD	5M570	??? Defined by user code. EPT-Transfer-Demo code: 50mA	??? Defined by user code. . EPT-Transfer-Demo code: 50mA
Bus Transceivers	74LVC8245		15mA (All eight I/O's active)
USB Chip	FT2232H		60 mA (no sink current supplied to I/O's)

USB EEPROM	93LC56		2 mA (write current) 1 mA (read current)
66MHz Oscillator	CB3LV-3I-66M0		10 mA
Op-Amp driver	MCP6L04		0.5 mA (all four amps active)
Schmitt Buffer	74LVC1G17SE		1mA
User LEDs			20 mA
Total		**50mA**	**175.5mA**

*Theoritical Values only. This data needs to be validated

9.2 Core Board VUSB Power Budget

Device	**Part Number**	**VUSB**		
+1.8V Power Supply	MCP1725-1802E	70mA		
+3.3V Power Supply	MCP1725-3302E	215mA		
Total		**285mA**		

* Theoritical Values only. This data needs to be validated